# An Acoustic Charge Transport Imager for High Definition Television Applications

NASA Grant #NAGW-2753

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# Executive Summary: Second Semiannual Report

## An Acoustic Charge Transport Imager For High Definition Television Applications

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This report represents work done during the second six months of work on the DARPA/NASA sponsored project, "An acoustic charge transport imager for high definition television applications." This section presents a brief summary of those accomplishments.

Our primary goal thus far has been to establish the feasibility of developing an acoustic charge transport (ACT) imager for high definition systems applications. The proposed chip will consist of about 2 million pixels, each of which is comprised of a GaAs/AlGaAs superlattice avalanche photodiode (APD) as a sensor element and an overflow and charge transfer transistor to transfer the photogenerated charge into the ACT channel for readout. Herein we discuss our progress towards developing each of these three aspects of the chip.

Experimental work was conducted on thin piezoelectric films over a GaAs substrate. Specifically, we investigated surface acoustic wave (SAW) propagation characteristics and the piezoelectric coupling of ZnO films. These films were grown by two different groups at Motorola and though much work remains on this subject the results are promising. The best

results were obtained with a DC Triode sputtered 1.6 μm thick film over a 0.2 μm $Si_3N_4$ passivation layer. For this configuration the effective piezoelectric coupling was 10.8 times higher than what it is for bare GaAs and is close to that which our theory predicts. This would result in a reduction of the RF drive power for the SAW transducer on the ACT device of 10.3 dB thus increasing device lifetime and reliability and reducing the chip power requirements. The problems that remain to be evaluated are the SAW attenuation and the prospect that the Zn in the film will migrate and dope the GaAs substrate p-type. If these problems are worked out this will represent a significant contribution to ACT device technology in general.

We developed a measurement system capable of full characterization of ACT devices for both imaging and communication systems applications. When the imaging applications of the ACT device are of interest the system will be used to characterize charge transfer efficiency, point spread function and charge capacity. For RF signal processing applications, gain, noise figure and distortion can be measured. A variety of measurements were made on a number of ACT devices. We also developed a small-signal circuit model for ACT devices. The model includes noise sources so that predictions of noise figure and/or charge packet variance can be calculated. It has advantages over previously reported models in that it is easily implemented on commercially available circuit analysis software. The mode provides a good compromise between computationally intensive field solvers and faster, but less accurate behavioral models.

Numerous material growth and fabrication procedures unique to this project were enhanced and a variety of devices were fabricated. Considerable work was done on the development of the charge transfer and overflow transistor and it is anticipated that results

will be forthcoming within the next two months. In addition work progressed with the APD devices and the ACT devices. APD uniformity measurements are being made and the preliminary results are promising.

Within the theoretical program there were principally two areas of development. One involved the development of a three-dimensional coupled drift-diffusion and Poisson equation solver useful for designing and evaluating the charge transfer and overflow transistor. We succeeded in producing a three dimensional drift-diffusion-Poisson solver which can be used to study any junction type. It has been shown that this model can correctly handle all of the features included within the transistor. This will be a valuable tool as we interpret the experimental measurements and seek to optimize the transistor performance. The other part of the theoretical program involved the APD development. We are developing a more refined version of our model for impact ionization which includes the full details of the band-structure for both the conduction and valence bands as well as the full order calculation of the phonon scattering rates providing a state-of-the-art determination of high energy transport. Upon its completion, the refined model will enable a better means for predicting the performance of the APD structure and a more accurate means for enhancing the design.

# AN ACOUSTIC CHARGE TRANSPORT IMAGER FOR HIGH DEFINITION TELEVISION APPLICATIONS: SECOND SEMIANNUAL REPORT

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## ABSTRACT

In this report we present the progress during the second six month period of the project "An acoustic charge transport imager for high definition television applications." This includes both experimental and theoretical work on the acoustic charge transport (ACT) portion of the chip, the theoretical program modelling of both the avalanche photodiode (APD) and the charge transfer and overflow transistor and the materials growth and fabrication part of the program. These areas are discussed respectively in Sections I, II and III.

# I. Work Accomplished During This Period: ACT Devices

## 1. Surface Acoustic Wave Properties of ZnO Films on {100}-Cut <110>-Propagating GaAs Substrates

GaAs has been employed as a material for ACT devices because it is a piezoelectric semiconductor. However, because GaAs is such a weakly piezoelectric material, the surface acoustic wave (SAW) interdigitated electrodes (IDT) drive power required to achieve charge transport is typically about 27 dBm. An enhancement of the piezoelectric coupling could potentially improve device lifetime, reliability, dynamic range and decrease power consumption. The length of the IDT and the reflector (which reflects the backward propagating wave to enhance the forward propagating power) also may be reduced, resulting in the reduction of the device size. To this end we are investigating the use of ZnO films and AlN films on top of the ACT substrate to enhance the piezoelectric coupling. In addition, these piezoelectric films would make it possible to construct monolithic devices with ordinary SAW devices and GaAs electronics. Herein we will discuss our progress on ZnO films. Within the next month we should receive the AlN films from Bell Northern Research and similar studies will commence on those films. In order to provide a basis for the design of such devices, we are investigating the SAW properties, including effective piezoelectric coupling constant, slowness surface, and propagation loss, measured on sputtered ZnO films over {100}-cut <110>-propagating GaAs substrates.

Over the past two decades, ZnO films have been the most frequently considered amongst various piezoelectric thin films used to increase the piezoelectric coupling in the case of a weakly piezoelectric or non-piezoelectric substrate material [1]. Knowledge of the SAW properties of the aggregate structure is critical for optimum design. The feasibility of ZnO

film for ACT devices has been predicted theoretically by Kim and Hunt [2]. There have been a few experimental papers of ZnO film on GaAs substrates [3]-[5], but the amount of the information about the acoustical properties is not sufficient to apply to the design of ACT devices or monolithic SAW devices.

For our work we have performed measurements on different thicknesses of ZnO films over the range of 1.6-4 μm and with films of different grain sizes. IDTs operating between 180 and 360 MHz were fabricated, and a laser probe was used to measure the SAW propagation. In addition, several multichannel waveguides were fabricated on the same substrates, and the measurement and the evaluation will also be performed for these devices. The measured data is compared with theoretical predictions.

We will report measured SAW properties, such as slowness surface, $K^2$, attenuation on the 1.6 μm thicknesses of ZnO films over semi-insulating {100}-cut <110>-propagating GaAs substrates for the frequency range of 180-360 MHz. For applications to ACT devices, we might need passivation layers such as $SiO_2$ [4], $Si_3N_4$ [6], or SiON [7] in order to: 1) passivate the structure and enhance the yield, 2) prevent unnecessary doping of GaAs by Zn during subsequent fabrication processes. The application of such passivation layer was also considered in this experiment with a $SiO_2$ for a $Si_3N_4$ layer. The results with and without the passivation layer will be compared with theoretical values.

## 2. ZnO Film Growth

The c-axis oriented ZnO films have been grown using both RF and DC triode sputtering method on {100} cut GaAs wafers provided by LEC crystal growth. The GaAs wafers are semi-insulating with resistivity $\geq 10^7\Omega$-cm, and the surface normal direction is (100) ±0.1°. The quality of the film strongly depends on the fabrication conditions. The typical deposition parameters used for the ZnO film are listed in Table 1. The film thickness-

es have been chosen 1.6, 2.4, and 4.0 μm to cover the range of 0.1-0.5 of the acoustic wavelength. As a passivation layer, we have grown an 1000 Å PECVD $SiO_2$ layer for the RF sputtered ZnO films and an 1500 Å CVD $Si_3N_4$ layer for the DC triode sputtered films.

Table 1: ZnO Film Deposition Parameters

| System | RF Magnetron | DC Triode |
|---|---|---|
| Target | 6.5 inch dia. circular magnetron | Ceramic 4 inch dia. |
| Target to Substrate Distance | 1.5 inches | 3.5 inches |
| Background Pressure | 8 mTorr | 3 mTorr |
| Substrate Temperature | 350°C | 250°C |
| Gas | 82% Ar 18% $O_2$ | 90% Ar 10% $O_2$ |
| Power | 400 W | 150 W |
| Rate | 4.6 μm/hr | 1.4 μm/hr |

The as-grown ZnO films are transparent with a very smooth surface finish. The grain size of the ZnO films is 0.2-0.5 μm for the RF sputtered films, and no grain boundaries are visible under SEM examination for the DC triode sputtered films. The problem with the DC triode sputtered films, however, is that a compressive stress is induced in the substrate. The induced stress is greater with the thicker films where warpage of the wafer becomes more evident. Thus, we only were able to investigate 1.6 μm thickness for the DC triode sputtered films. The warpage, however, is not expected to be a problem for 3-inch wafers.

## 3. Experimental Procedure

A number of devices shown in Figure 1 have been fabricated using a standard lift-off process on 1.6, 2.4, and 4 μm thicknesses of the ZnO film. The device is designed so that the upper four IDTs in Figure 1 may be for the measurement of SAW properties, and the lower four for multichannel waveguides. Employing one set of four IDTs with different center

frequencies allows to investigate frequency characteristics of 180-360 MHz. The configuration of the IDTs are listed in Table 2. Each IDT was unapodized and had a metalization ratio

Table 2: Configuration of IDTs

| No. $i$ | Type | Wavelength ($\lambda_i$) [μm] | Center freq. ($f_c$) [MHz] | Aperture ($W_i$) | | Number of finger pairs ($N_i$) |
|---|---|---|---|---|---|---|
| | | | | [μm] | [$\lambda_i$] | |
| 1 | split | 16 | 180 | 80 | 5 | 50.5 |
| 2 | solid | 12 | 240 | 100 | 8.3 | 50.5 |
| 3 | solid | 10 | 280 | 100 | 10 | 50.5 |
| 4 | solid | 8 | 360 | 80 | 10 | 50.5 |

of 0.6. For ease of the fabrication, the critical dimension of the devices was restricted to 2 μm; therefore, the No. 1 IDT has split finger electrodes and the others have the single finger configuration. The values of the wavelength, $\lambda$, and the center frequency, $f_c$, in the table denote nominal values. The value of $\lambda$ implies the periodicity of the IDT electrodes, and the SAW velocity, $\upsilon_{SAW}$, may be obtained to first order by the relation, $\upsilon_{SAW} = f_c\lambda$. However, not only is it difficult to pick up the exact value of $f_c$ experimentally, but also the value of the nominal $\lambda$ is different from that of the actual $\lambda$ because $\upsilon_{SAW}$ is perturbed by the IDT structure at the IDT. Thus, the exact value of $\upsilon_{SAW}$ should be obtained from the acoustic wavelength measured directly by using our laser probe. The values of $f_c$ in the table are given assuming that the SAW velocity is 2880 m/sec. Of course, it should be noted that $\upsilon_{SAW}$ is dispersive for the filmed structure. The apertures of the IDTs were chosen to allow for measurements of the diffraction of the wave on bare GaAs substrates [8]. The number of finger pairs, N = 50.5, will make the fractional 3 dB bandwidth of the IDTs to be 1.8 by the relation [9]

$$BW_{3dB}\% = \frac{0.9}{N} \times 100\%.$$

Considering the resistivity of the metal sheet of the IDTs [10], we chose the metal thickness to be 1000 Å of Al/4% Cu alloy.

The effective piezoelectric coupling constants, $K^2$, is generally obtained by a relative shift in velocity between open- and short-circuited surface as follows,

$$K^2 = 2\frac{v_o - v_s}{v_o}$$

where $v_o$ and $v_s$ are the open- and short-circuited velocity, respectively. For the measurement of $v_s$, a metal pad, which is shown in the left side of the upper four IDTs of the Figure 1, has been evaporated to short out the electric field on the surface. In order to reduce the mass loading of the metal pad, it was fabricated with 250 Å thickness of A/4% Cu alloy. In spite of the finite thickness of the pad, its mass loading would be negligible because it has a very slight effect compared to the piezoelectric effect [11]. Acoustic absorber has been applied at the both ends of the device to the propagation direction in order to prevent reflections from the edges.

The attenuation, $\alpha$, of the SAW can be measured by comparing the energy contained in the wave of two different transverse scans, separated by some distance *d*. The energy is proportional to the amount by summing up the squared magnitude of the beam profile, $|U|^2$, along the transverse direction. We should make the scan length to be long enough to include the entire energy because the beam spreads out by diffraction. Thus, the attenuation is given by

$$\alpha = 10 \log \left( \frac{\sum_1 |U|^2 \delta x}{\sum_2 |U|^2 \delta x} \right) \left( \frac{\upsilon_o}{d} \right) dB/\mu s.$$

A knife-edge laser probe system was used to measure SAW properties. The use of the laser probe system and the scheme for the longitudinal and transverse scans has been described in References [11], [12] and will not be discussed here. Theoretical calculations of the values of $\upsilon_o$, $\upsilon_s$, and $K^2$ for the film thicknesses were performed using our previously developed Laguerre polynomial technique [13].

The center frequencies of the devices have been measured, and the SAW velocities obtained using the center frequencies are compared with the theoretical values in Figure 2. The laser probing of the devices is still in progress. We anticipate that we will learn a great deal from these experiments.

## 4. Development of a HACT Measurement System

We have developed a measurement system capable of full characterization of HACT devices for imaging and communications systems applications. When used for image multiplexing, time domain measurements, such as impulse response are used to characterize charge transfer efficiency (CTE), point spread function, and charge capacity. For signal processing applications, characterization in terms of gain, noise figure, and distortion are performed in the frequency domain. Both applications, as well as materials characterization require accurate DC characterization.

The measurement system we have developed is comprised of approximately $70 K of measurement equipment. An HP6114A Power Supply and an HP3468A DVM are used for DC characterization. A Tektronix TDS 620 Digital Storage Oscilloscope is used in conjunction with an HP8130A Pulse Generator for impulse response and CTE measurements as shown in Figure 3. An HP8753B Network Analyzer is used for frequency response measure-

ments as shown in Figure 4. For distortion measurements, an HP8591A Spectrum Analyzer is used to examine frequency components of the distorted signal. This setup is shown in Figure 5. The same setup is also used for noise measurement. The SAW signal for the HACT device is generated by a time-stabilized HP8657A Signal Generator, shown in all of the test setups. Both the Network Analyzer and the Spectrum Analyzer are phase-locked to the stable reference on the HP8657A to increase measurement accuracy. In addition to these instruments, various power supplies, amplifier, filters, cables, attenuators, and adapters were purchased to aid in testing.

Using the equipment described above, we performed a number of measurements on a number of HACT devices. Figure 6 shows the measured impulse response of a 160 tap HACT device using the setup shown in Figure 3. The measured frequency response of a 160 tap HACT device is shown in Figure 7 using the setup shown in Figure 4. Figure 8 shows intermodulation distortion measurements on a 160 tap device using Figure 5.

Future plans include automating the various test setups using Lab Windows to control the instruments over an IEEE-488.2 bus. This will allow rapid testing of multiple devices to identify critical process parameters. The accuracy of noise figure measurements will be improved by implementing a Y-factor measurement with a controlled noise source. Further refinements in impulse response are being investigated by stabilizing charge injection with SAW frequency.

## 5. Development of a Small-Signal Circuit Model for HACT Devices

In order to accurately predict the behavior of HACT devices in both imaging and communication systems, we have developed a small-signal circuit model. This model includes noise sources so that predictions of noise figure and/or charge packet variance can be calculated. It has advantages over previously reported models in that it is easily implemented

on commercially available circuit analysis software. The model provides a good compromise between computationally intensive field (Poisson) solvers and faster, but less accurate behavioral models that have been proposed.

The model is broken into three sections based on the functional processes that occur in HACT devices: input charge injection, charge transport, and output sense. The injection process is linearized in such a way that an input signal sample can be represented as either a charge packet or an equivalent channel current. The former is preferred for imaging applications, while the later is best suited for signal processing applications. This model was implemented on Libra™, a commercially available microwave circuit analysis program. The predicted versus measured frequency response is shown in Figure 7.

Noise is associated with each process in the HACT device: input, transfer,and output noise. Input and output noise arises from the thermal noise of these structures. Transfer noise results from the random trapping and emission of carriers in interface states. Depending on the device architecture, any one of the three can dominate the noise performance. We compared the model prediction of midband noise figure to measured noise figure obtained from the setup shown in Figure 5, and to previously published HACT noise figure data. The predictions were in good agreement with less than 5% error. Table 3 shows the measured and calculated midband noise figures for a group of HACT devices, and their respective errors.

We expect to improve the accuracy of the noise figure measurement by using a Y-factor measurement. This will simultaneously measure associated gain and noise figure. We also plan to extend the model to include nonlinear effects such as charge capacity limitation and finite-width sampling aperture.

Table 3: Measured and Calculated HACT Noise Figure

| Configuration | Calculated NF | Measured NF | % Error |
|---|---|---|---|
| 20 Tap | 17.3 | 16.5 | 4.6 |
| 160 Tap, Low gm | 17.5 | 17.7 | 1.0 |
| 160 Tap, High gm | 17.0 | 16.5 | 2.9 |
| 320 Tap | 17.0 | 16.5 | 2.9 |

# II. Work Accomplished During This Period: Theoretical Program

## 1. Transistor Development

During the phase zero year of work, we have developed a three dimensional coupled drift-diffusion and Poisson equation solver useful for designing and evaluating the charge transfer, overflow and storage transistor. The specific tasks completed are:

(1) Completed the development of a standard three dimensional drift-diffusion solver

(2) The solver has been tested:

  (a) to analytical models to ensure accuracy

  (b) two-dimensional solution

  (c) compared to standard two-dimensional solvers - excellent agreement has been attained

  (d) extended to three dimensions and tested

(3) Structures containing the essential features of the charge transfer, overflow and storage transistor have been examined. A flow chart showing how the numerical simulation of the transistor is structured is shown in Figure 9. The first step in the procedure is to discretize the partial differential equations and solve them on a simulation domain. The discretization is performed using the finite difference method along with the Scharfetter-Gummel technique to ensure convergence. This results in a large system of non-linear algebraic equations. The resulting system of equations is solved using the biconjugate gradient squared method with appropriate preconditioners. Specifically, we have chosen to use the incomplete Cholesky decomposition. This choice, is in our opinion,

the most appropriate approach since it enables ready extension to the hydrodynamic method which will be developed during the next year of work. Once the equations are solved, an error comparison test is performed. If the error is sufficiently small, the solution is retained and the result is output. If the error is still too large, additional iterations are performed until it converges.

The simulator has been tested on various model devices. In this report, we will discuss three separate tests. The first test device is a simple p-n silicon homojunction diode. The device consists of n and p type layers doped at $1.0 \times 10^{17}$ $cm^{-3}$. The structure is reverse biased at -1.0 V. The potential along the central axis of the device is calculated both numerically (using the computer simulator discussed above) and analytically, using a one dimensional approximation. Comparison of the analytical and numerical solutions of the potential within the device are shown in Figure 10. As can be seen from inspection of Figure 10, the numerical calculation agrees with the analytical formulation precisely over the full length of the depletion region. The two dimensional solution for the potential in this structure is shown in Figure 11. As can be seen from Figure 11, the potential is well behaved throughout the depletion region as expected.

The second device tested consists of two p-n homojunctions arranged as shown in Figure 12. Homojunctions are formed at each interface between the different materials. This structure is of importance to study since the proposed charge collection, transfer and overflow transistor contains overlapping p and n layers in much the same fashion as in the structure shown in Figure 12. Therefore, it is important that our simulator be able to accurately handle these types of structures. As in the first test device, the dopings of the n and p layers are $1.0 \times 10^{17}$ $cm^{-3}$. In this case the material system is GaAs. The equilibrium solution for the potential is first calculated. The result is displayed in Figure 13. A reverse bias is applied

across the structure as shown in Figure 12. The calculated potential under these conditions is shown in Figure 14. As can be seen from comparison of Figures 13 and 14, the application of the reverse bias increases the band bending within the junctions.

Finally, since the proposed device contains an n-n heterojunction, our simulator must be able to accurately evaluate their performance. Our model includes not only drift and diffusion currents but also thermionic emission across the heterobarrier. It is well known that thermionic emission contributes significantly to the current flow in heterojunctions. We have examined a test diode which contains an n-n heterojunction between AlGaAs and GaAs, doped at $1.0 \times 10^{17}$ $cm^{-3}$ and $1.0 \times 10^{14}$ $cm^{-3}$. The conduction band bending calculated using the numerical simulator within the heterojunction is sketched in Figure 15. As can be seen from Figure 15 an energy band diagram typical of modulation doped heterostructures is obtained as expected.

In summary, the theoretical work during the zero phase effort has succeeded in developing a completely working three dimensional drift-diffusion-Poisson solver which can be used to study any junction type. It should be noted that our simulator has shown that it can correctly handle all of the features included within the transistor. In the near future we will begin analyzing the performance of the proposed charge transfer, collection and transfer transistor. In order to determine its performance we will first ascertain what physical parameters, i.e. charge capacity, leakage currents, etc., can and will be measured experimentally. Once we have decided exactly which measurements will be made on these transistors and how they will be performed, the simulator will be tailored to output these quantities. As a result, the simulator will help us to understand the workings of the transistor, interpret the experimental measurements, and enable a means of redesigning different features in order to optimize performance.

## 2. APD Development

During the first year of the zero phase program, we have been working on improving our existing simulators for calculating the electron and hole impact ionization coefficients. Our original models all rely upon an approximate formulation of the impact ionization transition rate. This formulation, commonly referred to as the Keldysh formula, is derived assuming parabolic energy bands, and fails to reflect any dependence of the ionization transition rate on the incident electron's k-vector. Preliminary studies [14-16] in various materials systems ranging from GaAs to GaInP indicate that the ionization rate is strongly dependent on the incident electron k-vector. Therefore, we have reformulated the impact ionization transition rate taking into account the k-vector dependence of the initiating carrier and including the full details of the overlap integrals and band structure.

Most studies of impact ionization use the Keldysh formula in order to determine the transition rate. The most commonly employed approaches use the ensemble Monte Carlo technique in conjunction with the Keldysh formula to calculate the carrier ionization rate. We have developed such a model and have employed it extensively to study carrier ionization in bulk material, heterostructures and multiquantum well devices. Our Monte Carlo model includes the full details of the band-structure for both the conduction and valence bands as well as the full order calculation of the phonon scattering rates providing a state-of-the-art determination of high energy transport. However, as mentioned above, it is likely that owing to the failure to include the wavevector dependence in the ionization transition rate that the impact ionization calculations based on the Keldysh formula are not entirely accurate. Therefore, in order to improve the accuracy of our Monte Carlo model we are working at including the wavevector dependence of the ionization rate.

The ionization transition rate can be determined from Fermi's Golden Rule as,

$$W_{imp} = \int \frac{2\pi}{\hbar} |M|^2 \, \delta(E_f - E_i) \, dS_f$$

where the matrix element, M, is defined as,

$$M = \frac{e^2}{\epsilon V} \frac{I(k_1, k_1') \, I(k_2, k_1')}{|k_1 - k_1'|^2 + q_0^2}$$

The terms $I(k_1,k_1')$ and $I(k_2,k_1')$ are the overlap integrals and $q_0$ is the screening factor. If the E(k) relation is assumed parabolic and the overlap integrals are approximated as constants, the transition rate can be evaluated analytically. The result obtained is the Keldysh formula given as,

$$W_{imp} = W(E_{th}) \, p \left[ \frac{E - E_{th}}{E_{th}} \right]^2$$

where $E_{th}$ is the ionization threshold energy, $W(E_{th})$ is the phonon scattering rate at the threshold energy, and p is a constant. The factors $E_{th}$ and p are determined by comparing the calculation to experiment. Therefore, the use of the Keldysh formula requires that the material be studied experimentally first such that the calculation can be compared to experiment and the parameters p and $E_{th}$ be determined.

One of the principal advantages of our new approach is that it does not rely upon the experimental evaluation of the ionization coefficients. In other words, the calculation requires no adjustable parameters and provides an essentially first principles evaluation of the ionization rate.

Rather than make the assumption of parabolic energy bands, we use a k•p calculation of the band-structure to determine the energy and wavefunction for any point within the first Brillouin zone. The transition rate is calculated at 916 mesh points within a three dimensional reduced zone (1/48 th of the entire zone) in the first Brillouin zone. Owing to the 48-fold symmetry of the crystal, once the transition rate is known within the reduced zone it is known

everywhere within the first Brillouin zone. A flowchart depicting how the transition rate is determined is shown in Figure 16. Basically, the transition rate is determined using a numerical integration. We have found that the best method, which affords high accuracy, is to numerically evaluate the integral by methodically selecting the final states throughout the first Brillouin zone. It is important to note that the full Brillouin zone must be sampled for the final states, otherwise the full range of angles appearing in the denominator of the matrix element will not be included. We have also tried to evaluate the matrix element using Monte Carlo integration but have found that this technique does not provide sufficient accuracy.

The initial state, denoted by $k_1$ and $E_1$, is chosen from one of the 916 mesh points. The final state, $k_1$' is chosen randomly and its energy, $E_1$' is determined from the k•p calculation. If the final energy plus the energy gap exceeds the initial energy, energy conservation cannot be preserved and the final state is prohibited. Another final state, $k_1$' is then selected. This procedure continues until the energy condition is satisfied. Then the final state of the generated electron, $k_2$', is chosen and its energy, $E_2$' is determined from the k•p calculation. Again the energy conservation condition is examined. If the sum of the final state energies and the energy gap are greater than the incident electron energy, new final states are selected. If the energy conservation condition is satisfied, the initial state of the target electron, $k_2$, is determined from the conservation of momentum. Its energy is determined and the energy conservation condition is once again examined. Provided that the final energy equals the initial energy, the process can occur. The overlap integrals are then evaluated directly using the values of the wavefunctions calculated from the k•p formulation. This procedure is continued until all of the final states within the first Brillouin zone have been sampled.

The major limitation of the above approach is that it is highly computer intensive. Unfortunately, to determine the transition rate for the desired number of points at the accuracy required, it will take an additional two months of computing. Presently, we are in the midst of this calculation. Once the transition rate has been determined, it will be included into our existing ensemble Monte Carlo electron simulator and the impact ionization rate in bulk GaAs will be recalculated and compared to experiment. Then the ionization rate will be recalculated in heterostructure devices and in the doped quantum well APD devices to be used in this project.

Additional theoretical work is in progress on refining the hole simulator. As is well known, the valence bands within III-V compound semiconductors are highly warped making the use of the parabolic approximation, even at low energies, highly suspect. Most existing hole simulators utilize the effective mass approximation in calculating the hole-phonon scattering rates as well as the Keldysh formula. We are developing a new approach in which the phonon scattering rates are determined numerically for all points within the Brillouin zone in much the same manner as discussed above for the impact ionization transition rate. This work is presently underway and results will be available soon.

Using the refinements discussed above, our ensemble Monte Carlo simulators will provide the most sophisticated means of predicting the impact ionization rate in compound semiconductors and semiconductor devices. We expect that these simulators will be finished during the first year of the follow-on funding of the project. Upon their completion, the proposed APD structure will be reexamined and its ultimate limits of performance more accurately assessed. In addition, these new refined models will enable a better means of designing these structures and a much more accurate prediction of their performance.

# III. Work Accomplished During This Period: Fabrication and Materials Growth

## 1. Molecular Beam Epitaxy of GaAs/AlGaAs Heterostructures

The epitaxial layers were grown in a Varian Gen II III-V MBE system. Careful calibration of the growth rate for GaAs was carried out by observation of RHEED intensity oscillations. The growth rate was set at 0.5 ML/S and monitored routinely, and typical was stable to within less than 1% over several days. The growth was carried out under arsenic stable conditions at 580°C to reduce any dopant diffusion or segregation. Generally, a 0.25 μm thick semi-insulating layer of GaAs or a short period superlattice structure of GaAs/AlGaAs was grown as buffer to smooth the growth surface and reduce the migration of substrate defects into the epilayer.

GaAs layers were doped with Si or Be to obtain n or p layers. The Si and Be sources were calibrated by growing 1 um thick layers and measuring their carrier concentration by either Hall effect or C-V. The former gives precise doping concentrations to within 3%. The electrochemical C-V profiling provides both doping concentration data, and also a profile of the ionized impurities (dopants) as a function of depth, thus also a verification of the growth rate. Figures 17 and 18 show profiles of samples B92-55 and B92-56 as grown by MBE and measured by Polaron. These samples were intended for ion implantation evaluation. Sample B92-55 has a 0.5 μm of Si doped GaAs at 1 x $10^{18}$ $cm^{-3}$ and is capped with 400 Å of GaAs doped at 5 x $10^{18}$ $cm^{-3}$. Sample B92-56 has a similar structure but is doped with Be. The profiles show the precision of doping and layer as well as the accuracy of the polaron technique. The reason for the gradual decrease in carrier concentration at around 0.4 μm is

that the underlying layer is semi-insulating and hence the depletion depth becomes larger as etching is continued and the measured point approaches the intrinsic layer.

To assume that the precise doping densities and layer thickness required for HACT structures were obtained as intend, we have designed an additional doped layer structure as shown in the insert of Figure 17. On a Si doped GaAs substrate, we have grown 0.1 μm of i - GaAs, followed by 0.1 μm -5 x $10^{17}$ $cm^{-3}$, 0.1 μm of -3 x $10^{17}$ $cm^{-3}$, 300 μ of -3 x $10^{17}$ $cm^{-3}$ and 2 x $10^{17}$ $cm^{-3}$, 0.1 μm of -3 x $10^{17}$ $cm^{-3}$, and 0.1 μm of -5 x $10^{17}$ $cm^{-3}$. The intent here was to show that in the 300 Å region we could obtain precise compensation of donors and acceptors to create a layer of 1 x $10^{17}$ $cm^{-3}$ donors. This may be the only was to measure low dopant density and thin layer thickness simultaneously by the polaron measurement. For the data presented in Figure 19, the Be doping is clearly at 2 x $10^{17}$ $cm^{-3}$, compensated region at 1 x $10^{17}$ $cm^{-3}$. Thus, very accurate doping profiles are possible by MBE we also expect this technique to be very useful in analyzing low doped ion-implanted wafers.

Various structures of n or p, np and pn doped layers were grown for both acoustic transport devices and ion implantation evaluation as described in the respective sections.

## 2. Material Evaluation

Special procedures were also developed to improve and maintain the accuracy and reproducibility of the evaluation techniques as described below.

The electrochemical C-V profiling involves C-V measurement at the constant voltage. The Schottky contact is made between the sample and a etchant liquid through an small diameter. The ohmic contact is made by direct contact of a metal probe into the surface. This contact must have a low resistance for the C-V evaluation to be valid. The C-V evaluation is carried out one point at a time as in conventional C-V, but after each measurement a few (2) nanometers of the sample were etched and then another measurement made.

This method of evaluation provides a powerful technique for obtaining the concentration of electrically active dopants to nearly any depth. Along with the dopant profile one also obtains I-V, C-V, and the conductance of the sample.

Some of the samples were also measured by conventional C-V profiling. The conventional C-V technique involves deposition of a metal on to the surface of the sample and the formation of a small area Schottky contact and a large area ohmic contact to the sample. In our experiments we used 150 μm diameter dots and a AuGe Schottky barrier. By placing a voltage on the Schottky contact and ensuring the depletion width and capacitance of the device we obtain the carrier concentration in the layer. Decreasing the voltage from zero produces larger depletion width and hence the carrier concentration at different depths of the sample can be measured. This technique only works for relatively shallow depths before I-V breakdown occurs.

## 3. Ion Implantation and Annealing Study for CTD

### 3.1 Device Concepts

The proposed charge transfer and overflow transistor devices are shown in Figure 20. The first design features an n-p-n GaAs bipolar transistor grown epitaxially onto the APD structure in which the n-type emitter region serves as the collector for charge output from the APD. The base region is comprised of two concentric p-type doped regions differing in the degree of p-type doping. The more highly p-type doped center region separates the n-type emitter and ACT channel layers. The more lightly p-type doped outer region separates the emitter from the overflow contacts. In the second design the base region is in the mesa and thus only a p-type implant is needed.

## 3.2 Material and Processing Procedures

In the test structures currently being investigated the device is grown by MBE using the following steps. First an n-type AlGaAs layer is grown on an n-type GaAs substrate to mimic the $n^+$ electrode of the APD. This is followed by the growth of a low-defect 0.2μm thick n-type GaAs layer doped to 2 - $6x10^{16}$ $cm^{-3}$ with silicon to form the holding well for the amplified photo-charge. This layer is then capped with a 0.2 μm thick p-type doped GaAs layer doped between 2 - 6 x $10^{16}$ $cm^{-3}$ to form the containing barrier and is followed by a 0.2 μm thick n-type GaAs cap layer which simulates the ACT structure.

For this npn transistor to perform both overflow and charge injection functions conventional photolithography and ion-implantation techniques are used to fabricate the mesa design shown in Figure 20. First the top n-type layer must be patterned to protect the ACT structure and the remainder of the n-type layer removed by conventional etching to expose the p-type base layer. This surface is then covered so as to expose only a 2 - 4 μm wide circular annulus around the top mesa for ion-implantation. To produce the transistor design required for this program requires a two stage ion-implantation process in which an annulus of the lowest n-type layer, is converted to a p-type layer using a multi-energy buried Be implant. By careful adjustment of the ion implant energy it is expected to localize the implanted Be close to the n-type GaAs layer and to minimize straggle and associated lattice damage. Fortunately, because of its light mass the buried Be implant is not expected to cause much damage. A second implant of Si will then be applied in the same region to effectively compensate and reduce the hole concentration in the p-type layer to close to that of the hole concentration produced by the Be implantation. Again to minimize straggle and damage a multi-energy implant will be used.

The fabrication of the CTD structure therefore requires that the following processes be developed.

(a) MBE growth of n-, p-type and n on p-type GaAs layers with doping between 2 and 6 x $10^{16}$ and 1 x $10^{18}$ cm.

(b) Determination of the electrical characteristics of beryllium and silicon implanted n- and p-type GaAs layers.

(c) Develop a test mask set and the fabrication processes for this device concept.

(d) Fabricate and evaluate prototype device structures.

The specific details of each of these tasks is given below.

## 3.3 Molecular Beam Epitaxy of GaAs

The samples were grown by MBE at 580°C on semi-insulating GaAs wafers under As stable conditions at a growth rate of 0.5 monolayers/sec. A thin 0.1 μm thick layer was grown as buffer layer followed by the active layers which were n- and p-type doped 2 and 6 x $10^{16}$ $cm^{-3}$ with thickness ranging from 0.2 - 0.5 μm to match the ion implantation range. Growth was concluded by a 200 Å thick heavily doped layer to facilitate low resistance contacts to the sample. Table 4 lists the samples grown for the ion-implantation studies.

## 3.4 Ion Implantation and Annealing Study for Carrier Conversion of n- and p-type GaAs

The major objective of this study was to obtain carrier conversion and modification in n- and p-type GaAs layers with very precise p- and n-type doping and well defined dimension characteristics. Both are very important for the fabrication of charge transfer and overflow devices as to first order the carrier concentration controls the overflow voltage characteristic and the depth of the implant the isolation (dark current) behavior. Thus very uniform and abrupt doping characteristics are needed which in turn depend on the implantation profile,

Table 4: List of MBE Runs for Ion Implantation

| Run # | Layer Thickness (um) | Doping (cm-3) | Layer 2 Thickness (A) | Doping (cm-3) | Size Wafer |
|---|---|---|---|---|---|
| B92-28 | 0.5 | Be 2*10e16 | 200 | Be 3*10e18 | 1/4 |
| B92-29 | 0.5 | Si 2*10e16 | 200 | Si 3*10e18 | 1/4 |
| B92-30 | 0.5 | Si 2*10e16 | 200 | Si 3*10e18 | 1 |
| B92-31 | 0.5 | Si 2*10e16 | 200 | Si 3*10e18 | 1 |
| B92-32 | Be doped staircase for calibration | | | | |
| B92-33 | 0.5 | Si 6*10e16 | 200 | Si 3*10e18 | 1 |
| B92-35 | 0.5 | Be 6*10e16 | 200 | Be 3*10e18 | 1/4 |
| B92-36 | 0.5 | Be 2*10e16 | 200 | Be 3*10e18 | 1 |
| B92-37 | 0.2 | Si 2*10e16 | 2000 | Be 2*10e16 | 1 |
| B92-38 | 0.2 | Si 2*10e16 | 2000 | Be 2*10e16 | 1/4 |
| B92-53 | 0.5 | Si 6*10e16 | 200 | Si 3*10e18 | 1 |
| B92-54 | 0.5 | Si 1*10e16 | 200 | Si 3*10e18 | 1 |
| B92-55 | 0.5 | Si 1*10e18 | 400 | Si 5*10e18 | 1 |
| B92-56 | 0.5 | Be 1*10e18 | 400 | Be 5*10e18 | 1 |
| B92-57 | 0.5 | Be 1*10e18 | 400 | Be 5*10e18 | 1 |
| B92-58 | 0.5 | Si 1*10e18 | 400 | Si 5*10e18 | 1 |

activation efficiencies and diffusion characteristics of the implanted species.

The initial program direction was based on previous reports of ion-implanted FET transistors. This work showed that the electrical activation of the RTA wafers was higher than those annealed conventionally and the diffusion of the implanted dopants was minimized. Both are very important for these devices which involve very small geometries. Rapid thermal annealing (RTA) also minimizes the outdiffusion of arsenic so that neither encapsulation nor an As ambient was needed for the initial studies.

## 3.5 Experimental Design

The purpose of the ion implantation study was to establish the range of doses and energies necessary to fabricate the two device configurations described above. In the first device it is necessary to perform a buried Be implant through a 0.2 μm thick p-type layer into an n-type layer, and to convert it from $10^{16}$ - $10^{17}$ $cm^{-3}$ n-type to $10^{16}$ - $10^{17}$ $cm^{-3}$ p-type, followed by a Si implant into the 0.2 μm p-type layer to slightly lower its hole conductivity. In the second device configuration only a surface Be p-type implant is needed into an n-type layer.

Because the net carrier concentration can depend on both the activation efficiency and implantation damage which induces stoichiometric doping, studies were performed as a function of dose and annealing in both n- and p-type epitaxial GaAs to assess any such effects.

To design test layer geometries computer codes were used to estimate the implanted carrier concentration and profile before and after annealing. The ion implantation profiles are generated from a PROFILE CODE™ program from Implant Sciences, Inc. [17]. These profiles are equivalent to those generated by Monte Carlo programs and calculate the implanted atom distribution in GaAs as a function of implant energy, dose, and implant angle, and also the resultant diffusion profiles after thermal annealing.

Multiple implants with different doses and implant energies were used to obtain a homogeneous implant profiles. The final implant profile is the summation of each individual implant profile. For Be, 4 implants with energies from 30-160 KeV were used to obtain a 0.5 μm implant into GaAs wafers. For Si, the implant profiles are much narrower compared to Be, because Si is much heavier and thus 5 implants were required to obtain a smooth profile.

Double charged implants (400 KeV) were necessary to obtain a 0.5 μm implant depth for the heavier Si atom.

The PROFILE CODE™ was then used to calculate and predict the diffused implantation profile after RTA. For the Be implant annealed at 750°C the diffusion constant is 8.9 x $10^{-12}$ $cm^2$/sec [19]. This calculation predicts the redistribution of the implant profile after the anneal assuming a 100% activation. However, the actual activation efficiency must be experimentally determined and compared to the predicted profile.

### 3.6 Implantation, Annealing, Evaluation

After the MBE growth, the wafers were cut into 4 pieces and the orientation of the GaAs wafer noted for the implantation. The wafer was then implanted at a 7° tilt to reduce scattering from the wafer surface and channeling in the wafer during the implants.

After receiving the samples from Implantation Sciences, Inc. a series of rapid thermal anneals was performed to study the activation of dopant. For this initial study a capless RTA technique was developed [19]. An unimplanted GaAs wafer was first set directly onto the silicon support plate of the RTA system and the implanted GaAs wafer then placed face down onto the unimplanted GaAs wafer. This produced a sufficient As over pressure to minimize the As outdiffusion. The anneal chamber was then pumped down to $10^{-5}$ Torr, charged with $N_2$ ambient at 570 Torr, and the wafer annealed. The annealing conditions for Be implanted wafers were 750 to 850°C for 10-60 seconds; for the Si implanted wafers 850°C for 30-60 seconds. The anneal temperature was monitored from the back side of the implanted GaAs wafer and stabilized by a feedback loop.

Different anneal time and temperatures have been reported to obtain optimum RTA treatment for Be and Si implanted wavers [20-23]. For Be implants, the reported anneal temperature is from 750 to 850°C, and anneal time is from 2 to 30 seconds [20, 21]. For Si

implants, the anneal temperature is from 900 and 1000°C, and the anneal time is from 5 to 200 seconds [24, 25]. In this work, we found that the best heat treatment for our Be multi-implanted wafers is at 850 to 900°C for 10 to 20 seconds.

During the course of this study it was found that a better capless anneal was obtained by using thicker (heavier) GaAs wafers for the implantation. This increased the contact pressure between the two wafers and thus, produced a higher surface As pressure to suppress the outdiffusion of As from the implanted layer.

### 3.7 Evaluation and Results

After annealing the electrical profiles were evaluated by Polaron measurements and also C-V and Hall effect measurements when necessary. The following conditions were found to be critical to obtain high accuracy in the polaron measurements. Ideally, an ohmic contact resistance less than 400 ohms is necessary for obtaining accurate measurements and uniform etching conditions. Good ohmic contact was established by passing a current pulse through the wafer surface.

To establish the etching conditions the I-V characteristics of the p-n diode formed by the electrode n-type region and the p-type Be implant was first measured to establish the voltage limits for the G-V (and C-V) measurement so as to avoid the breakdown region. The G-V measurement provides the conductance curve of the diode and is used to select the etching voltage which should be set close to, or zero in the flat region of the conductance curve. This voltage was then used throughout the etching measurement that directly measures the activated implant profile. An example of the accuracy of the etching measurement is shown in Figure 2 (a) for wafer B92-30C after a 750°C anneal for 30 seconds. This profile is very close to the intended diffusion profiles shown in Figure 2 (b), which also shows individual implants profiles and the total implant distribution.

Table 5 lists the samples used in the implantation studies. For the Be implanted samples the best results were obtained for high doses in part because very good ohmic contacts could be made to the sample for the C-V measurements. For example, samples B92-30C and D showed high implant activation with profiles closely matching the intended profiles and dopings. However, samples B92-33 C and D exhibited broad profiles with doping densities 1.5 times those intended (see figures). These samples were implanted to a depth of 0.5 μm at 2 x $10^{18}$ $cm^{-3}$ (C) and 4 x $10^{18}$ $cm^{-3}$ (D). However, the measured profiles extend to beyond 1 um at 3 x $10^{18}$ $cm^{-3}$ and 5 x $10^{18}$ $cm^{-3}$. For the MBE grown sample B92-33B doped to 6 x $10^{17}$ cm-3 the polaron profile was well behaved and confirmed the desired profile indicating that the differences in these samples are either in implantation nonuniformities or annealing differences. Annealing at high temperature can cause high diffusion of implanted species, however the carrier concentration should then decrease as the profile broadens, because the total implants dose is constant. This and the accurate profiles measured for other samples indicate that the implantation process may be at fault and that a larger and more energetic dosage of Be could have been placed in these two samples.

Table 5: List of samples used in ion implantation and annealing study

| Wafer No. | Imp. Conc. ($cm^{-3}$) | Sub. Doping ($cm^{-3}$) | R.T.A. ($^0$C,s) | | Concen. Peak Eff. |
|---|---|---|---|---|---|
| B9230A-R1A | P: 6.0E16 | n = 2E16 | 750 | 30 | No Contact |
| B9230A-R1B | p: 6.0E16 | | | 30 | No Contact |
| B9230B-R1 | p: 1.8E17 | | | 30 | No Contact |
| B9230B-R5 | p:1.8E17 | | | 10 | No Contact |
| B9230C-R1 | p: 6.0E17 | | | 30 | 5.2E17, 88% |
| B9230C-R3 | p: 6.0E17 | | | 60 | 5.2E17, 88% |
| B9230D-R1 | p: 2.0E18 | | | 30 | 1.8E18, 90% |

| Wafer No. | Imp. Conc. ($cm^{-3}$) | Sub. Doping ($cm^{-3}$) | R.T.A. (°C,s) | | Concen. Peak Eff. |
|---|---|---|---|---|---|
| B9233A-R1 | p: 1.8E17 | n = 6E16 | 750 | 30 | No Contact |
| B9233B-R1 | p: 6.0E17 | | | | 5.0E17, 93% |
| B9233C-R1 | p: 2.0E18 | | | | 2.2E18, 110% |
| B9233D-R1 | p: 4.0E18 | | | | 4.5E18, 111% |
| B9234A-R1 | p: 1.2E17 | p = 6E16 | 750 | 30 | No Contact |
| B9234B-R1A | p: 3.0E17 | | | 30 | No Contact |
| B9234B-R1B | p: 3.0E17 | | | 30 | 3.2E17, 48% |
| B9234C-R1 | p: 6.0E17 | | | 30 | 7.0E17, 107% |
| B9234C-R5 | p: 6.0E17 | | | 10 | 4.8E17, 73% |
| B9234D-R1 | p: 2.0E18 | | | 30 | 2.1E18, 105% |
| B9253A | p: 1.8E17 | n = 6E16 | Destroyed in Implant | | |
| B9253B | p: 6.0E17 | | | | |
| B9253C | P: 2.0E18 | | Measurement in Process | | |
| B9253D | p: 4.0E18 | | Measurement in Process | | |
| B9254A | p: 1.8E17 | n = 2E16 | Measurement in Process | | |
| B9254B | p: 6.0E17 | | Destroyed in Implant | | |
| B9254C | p: 2.0E18 | | Measurement in Process | | |
| B9254D | p: 4.0E18 | | Destroyed in Implant | | |
| B9255A | p: 1.6E18 | n = 1E18 | 850 | 20 | No Contact |
| B9255A | | | 900 | 10 | 3.5E17, 84% |
| B9255B20 | P: 3.0E18 | | 850 | 20 | 6.5E17, 55% |
| B9255B20Z | | | 850 | 20 | 7.8E17, 59% |
| B9255B | | | 900 | 10 | 1.0E18, 66% |
| B9255B | | | 875 | 10 | 1.0E18, 66% |
| B9255C | p: 5.0E18 | | Measurement in Process | | |

| Wafer No. | Imp. Conc. ($cm^{-3}$) | Sub. Doping ($cm^{-3}$) | R.T.A. ($^0C$,s) | Concen. Peak Eff. |
|---|---|---|---|---|
| B9256A | p: 1.0E18 | p = 1.E18 | Measurement in Process | |
| B9256B | p: 3.0E18 | | Measurement in Process | |
| B9258A | p: 3.0E18 | p = 1.E18 | Measurement in Process | |

Samples B92-34 B, C, and D also showed reasonable hole concentrations to within 3%, 4%, 14% of the intended implanted doses. However, the large depletion width prevented accurate range information from being obtained. Sample B92-34 A was semi-insulating. This was attributed to a low carrier concentration of ~ $1.8 \times 10^{17}$ $cm^{-3}$. The polaron system requires for higher carrier concentrations to make reliable measurement.

The summary of these measurements is shown in Figure 22 which plots the measured carrier concentrations verses implant dose for wafers B92-30, B92-34, and B92-37. Notice that nearly 100% activation efficiency was obtained for most samples. The different slopes indicate the range of activation efficiencies for these wafers. These variations are due to differences in implantation, annealing, or measurement and need to be addressed further.

From this work, the best results were obtained for the Be wafers implanted higher than $5 \times 10^{17}$ $cm^{-3}$, in part because good ohmic contacts could be made to the sample to perform the Polaron measurements. Unfortunately the low dose implant wafers appear to be semi-insulating and hence inaccessible by Polaron measurements. In order to obtain lower contact resistances in the second study new designs with a high concentration surface $p^+$ layer were used as shown in Figure 23 for wafer B92-55A. The $P^+$ layer was obtained by implanting Be at a high dose for a very low implant energy of 7 KeV.

Finally, procedures for depositing $Si_3N_4$ by plasma enhanced by chemical vapor deposition (PECVD) were also investigated to provide a cap for the Be implants in the

proposed device structures. A Plasma-Therm 700 Series system was used and the plasma enhanced $Si_3N_4$ deposition performed in the vacuum chamber of the PECVD system, using the following conditions

| | | | |
|---|---|---|---|
| (1) | Temperature: | 300°C | |
| (2) | Pressure: | 0.9 Torr | |
| (3) | Power: | 30 Watts | |
| (4) | Gas Sources: | $NH_3$ | 3 sccm |
| | | $SiH_4$ (Silane) | 200 sccm |
| | | $N_2$ | 900 sccm |
| (5) | Deposition: | 98-100Å/min | |

## 3.9 Future Directions

The outcome of these experiments indicates that while implantation provides a way to control the doping densities in the lateral dimension, its precision in depth and dosage density has to be improved for device applications. In the moderate to high dose regime the technique works well but in the low ($< 5 \times 10^{17}$ $cm^{-3}$) dose regime we could not make accurate measurements although we expect the techniques to work.

The activation efficiency and diffusion of the implanted species depends on the implant dose, energy, annealing time and temperature and the quality of the epitaxial layer. Further control over these parameters and As outdiffusion are major objectives in the work. Further studies to optimize the activation efficiency at the lowest annealing temperature and annealing time will also improve control over the implanted dopant distribution. Also any dependence of the activation level on the dose needs to be investigated further in order to

obtain precise control over multiple implant designs. The damage recovery of the annealed wafers may also need further study since the level of activation does not directly indicate the damage recovery of the wafers.

To perform these characterizations, other measurements, such as SIMS and Hall effect will be used for the characterization of low doses and for the fabrication of low implant devices. Even though the Polaron measurement could not be used to measure low dosage wafers, the implant and activation study carried in this work still offered significant information toward understanding the physical properties of implanted material. This understanding is necessary to successfully fabricate the n-p-n charge transfer and overflow devices proposed in this project.

## 4. Charge Transfer and Overflow Transistor Design and Fabrication

### 4.1 Mask Design

The mask set for the charge transfer and overflow device was designed at Georgia Tech and fabricated by Precision Photo Mask. The six layer set consists of a mesa, top contact, base contact, via, air bridge, and passivation layers. Four different transistors sizes with contact diameters of 8, 10, 20, and 40 μm are stepped over the mask.

### 4.2 Fabrication Process

The process path developed for fabricating test charge transfer and overflow transistors is shown in Figure 24 and described more fully below.

Before fabrication the GaAs wafer was thoroughly cleaned by rinsing in trichloroethylene, acetone, and methanol. The surface was then swabbed with Microclean with a final rinse in DI water, methanol, and acetone. To prepare the wafer for the mesa etch and implantation

the wafer was coated with Shipley 1650J photoresist spun at 4000 RPM (5 μm thick) and baked at 110°C for 25 minutes. The mesa geometries were then defined by a 12 seconds exposure at 12.5 mW/cm$^2$ and the patterns developed for 45 seconds in Microposit 351 developer diluted 1:3.5 with water. The mesa patterns were then etched with a solution of phosphoric acid, hydrogen peroxide, and DI water (3:1:50) to isolate the devices on the substrate for ion implantation.

After ion implantation the photoresist defining the top contact was removed and the wafer coated with Shipley 1350J photoresist diluted 3:1 with thinner and spun at 5000 RPM to produce a 0.75 μm thick film. The photoresist was baked at 95°C for 25 minutes and the top contact layer exposed for 4.5 seconds at 12.5 mW/cm$^2$. The wafer was then soaked for 10 minutes in chlorobenzene and hard baked at 95°C for another 10 minutes to produce a lip on the photoresist to allow the metal to be lifted off the unwanted areas. The patterns are developed for 1 minute in diluted 351 developer. N-type ohmic contact metal consisting of 800Å AuGe (88/12), 100Å Ni, and 1000Å Au was then evaporated and lift-off performed. The metal was alloyed to form a low resistance ohmic contact using a 30s rapid thermal anneal at 365°C.

The base contact layer was processed using the same steps as for the top contact, but the p-type metallization was AuZn (95/5) and Au alloyed at 425°C for 1 minute.

The via layer photoresist was prepared with diluted 1350J spun at 5000 RPM and baked at 95°C for 25 minutes. The pattern was exposed for 4.5 seconds at 12.5 mW/cm$^2$, soaked for 10 minutes in chlorobenzene and baked for 10 minutes at 95°C. The pattern was developed for 1 minute and a layer of titanium and gold was deposited but not lifted off.

The wafer was then coated with the thicker 1650J photoresist and softbaked at 80°C for 25 minutes. The air bridge layer was exposed for 12 seconds at 12.5 mW/cm$^2$ and the pattern developed. The wafer was then electro-plated with 1μm of gold and the photoresist removed leaving the thin via gold and the thick air bridge gold exposed. The thin via gold was etched away and the layer of photoresist below it removed with poststrip, leaving a thick bonding pad connected to an air bridge.

A passivation layer of $SiO_2$ was next deposited by PECVD, and 1350J photoresist applied to the wafer and the passivation mask exposed for 4.5 seconds at 12.5 mW/cm$^2$. After the photoresist patterns were developed and the $SiO_2$ was etched in a solution of ammonium fluoride and hydrofluoric acid (6:1) to expose the bonding pads. The devices were then diced and ready to be tested.

## 4.3 Summary

This development concluded the initial research steps that were undertaken to develop the technology base for fabricating an operational CTD structure for testing, evaluation and refinement before integration into the complete HACT structure. Work is currently in progress to integrate these procedures in order to have a workable device within the next two months. Coincident with this program evaluation equipment is being set-up to evaluate device characteristics and performance. Coincident with these studies some of the variances found in these processes will be researched to improve their accuracy and reliability. For example this ion-implantation study.

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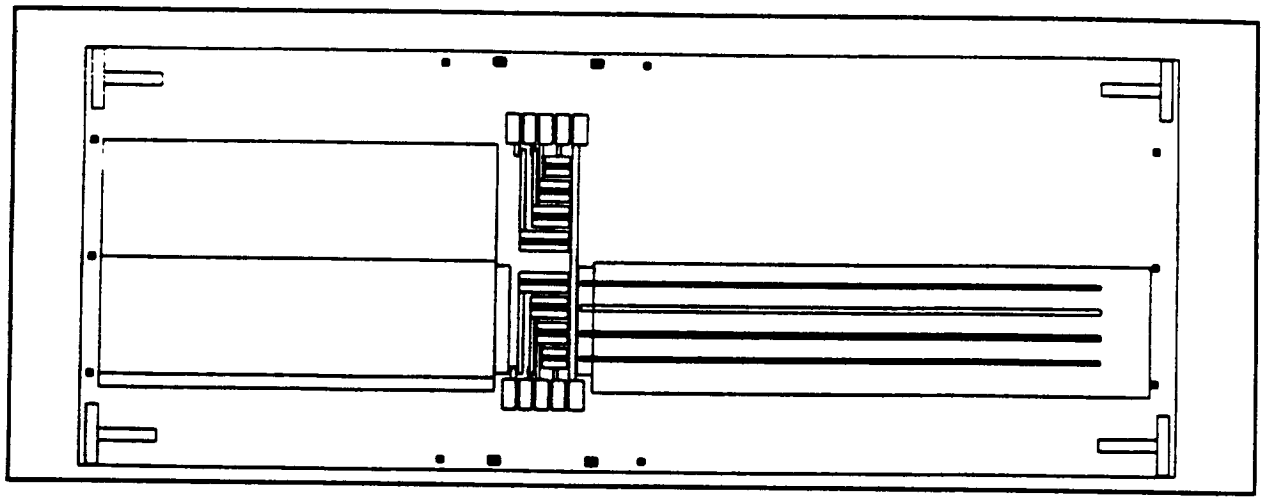

Figure 1: Device architecture for the measurements of SAW properties and waveguides.

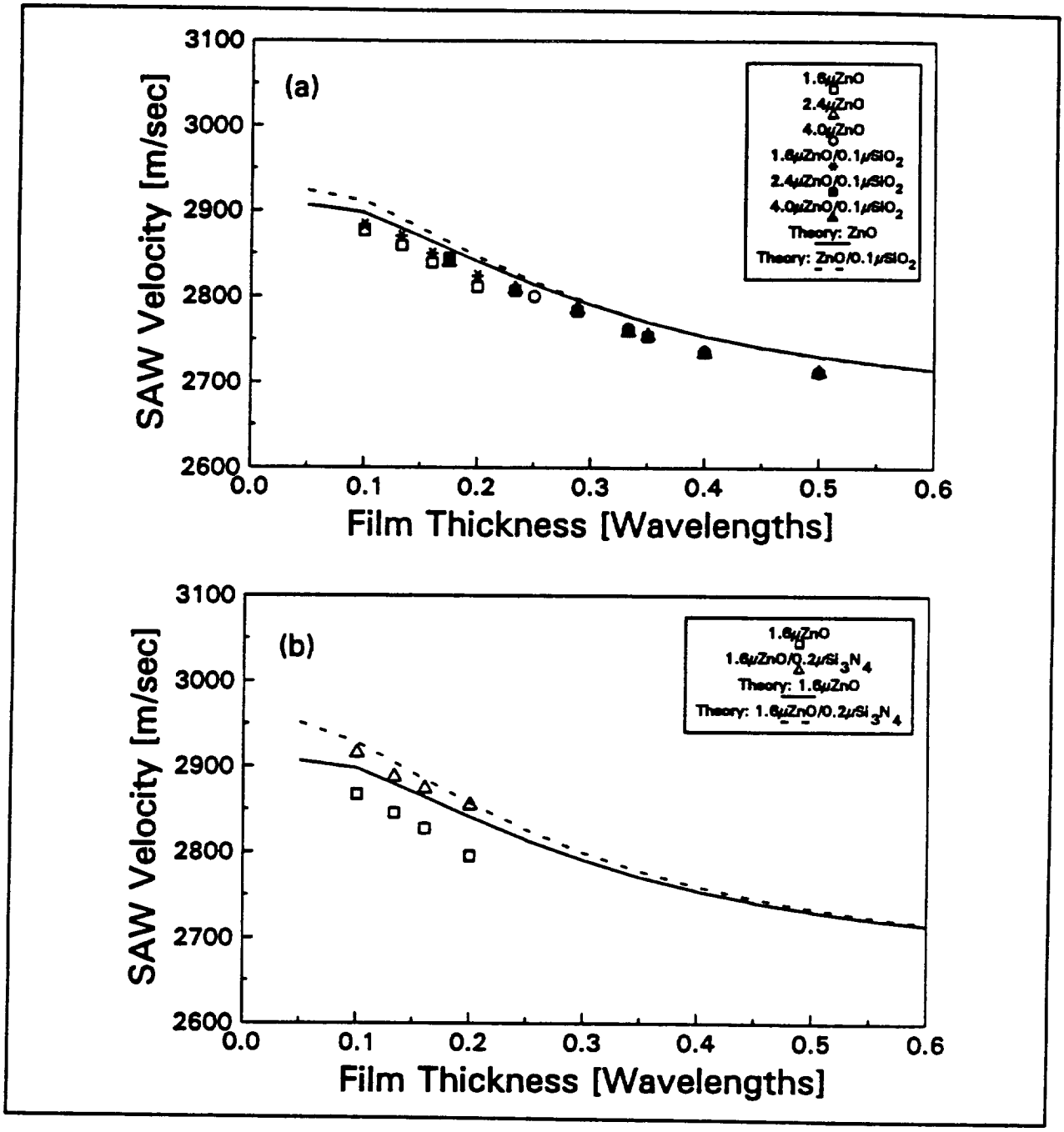


Figure 2: SAW velocities for AnO films on GaAs (a) RF magnetron sputtering and (b) DC triode sputtering.

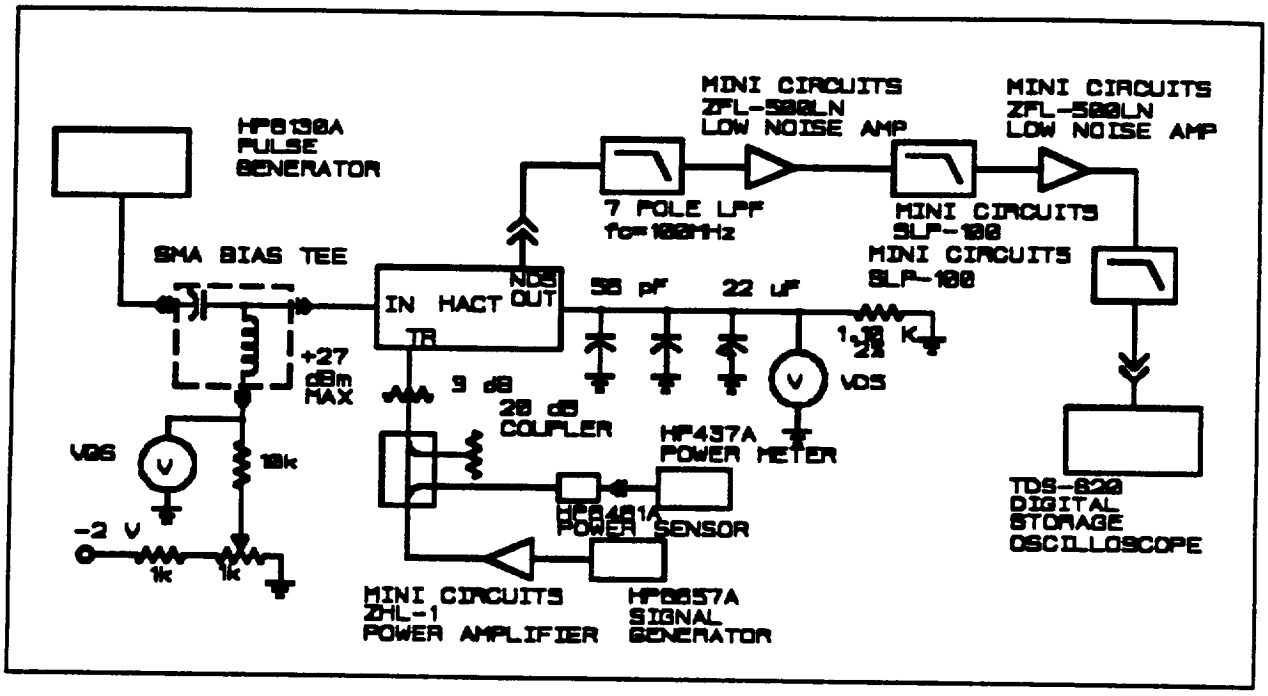


Figure 3: Transient response measurement setup.

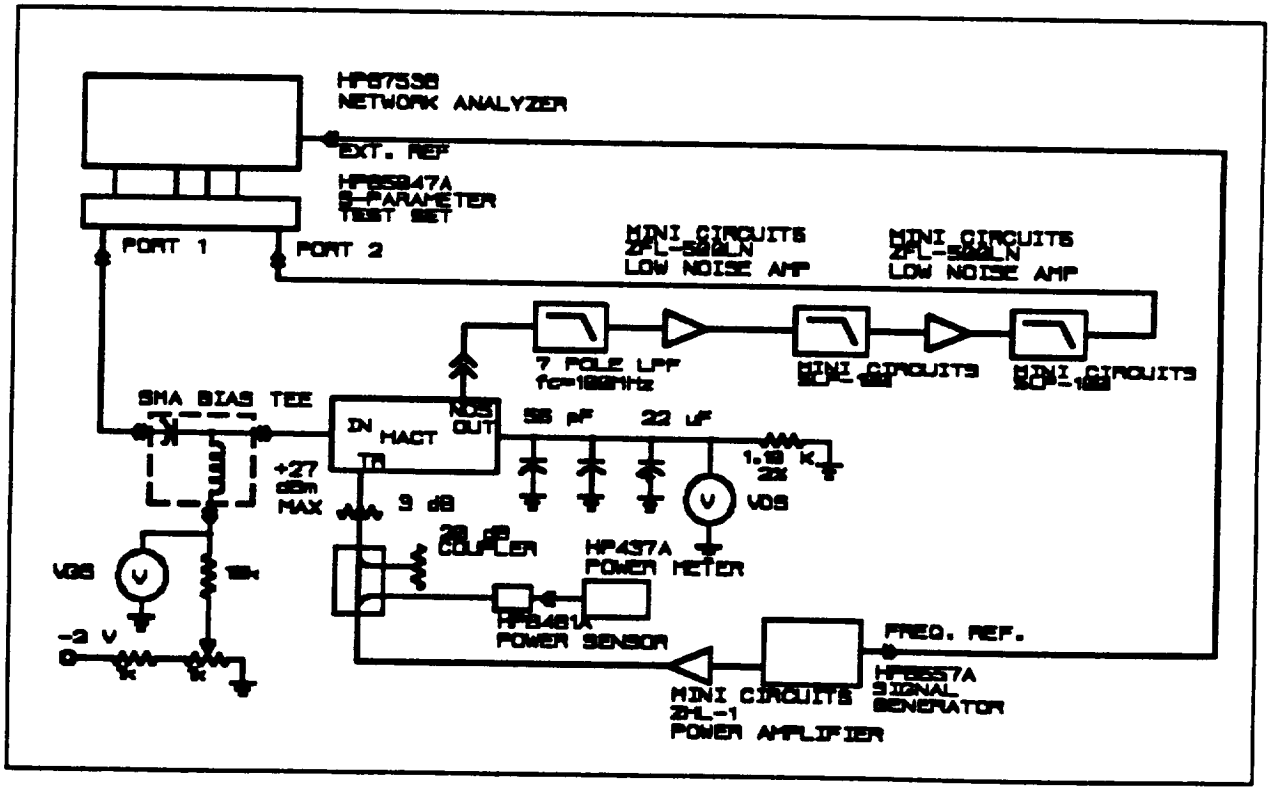


Figure 4: Frequency response measurement setup.

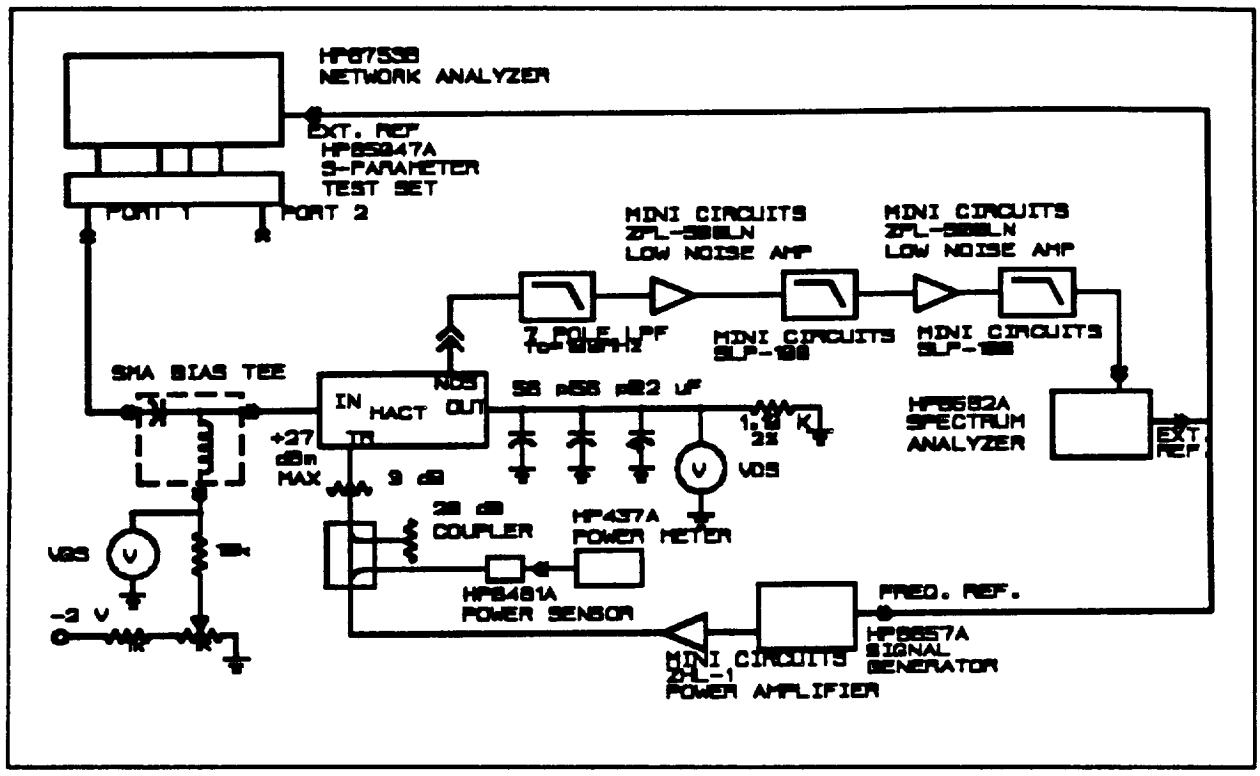


Figure 5: Distortion and noise measurement setup.

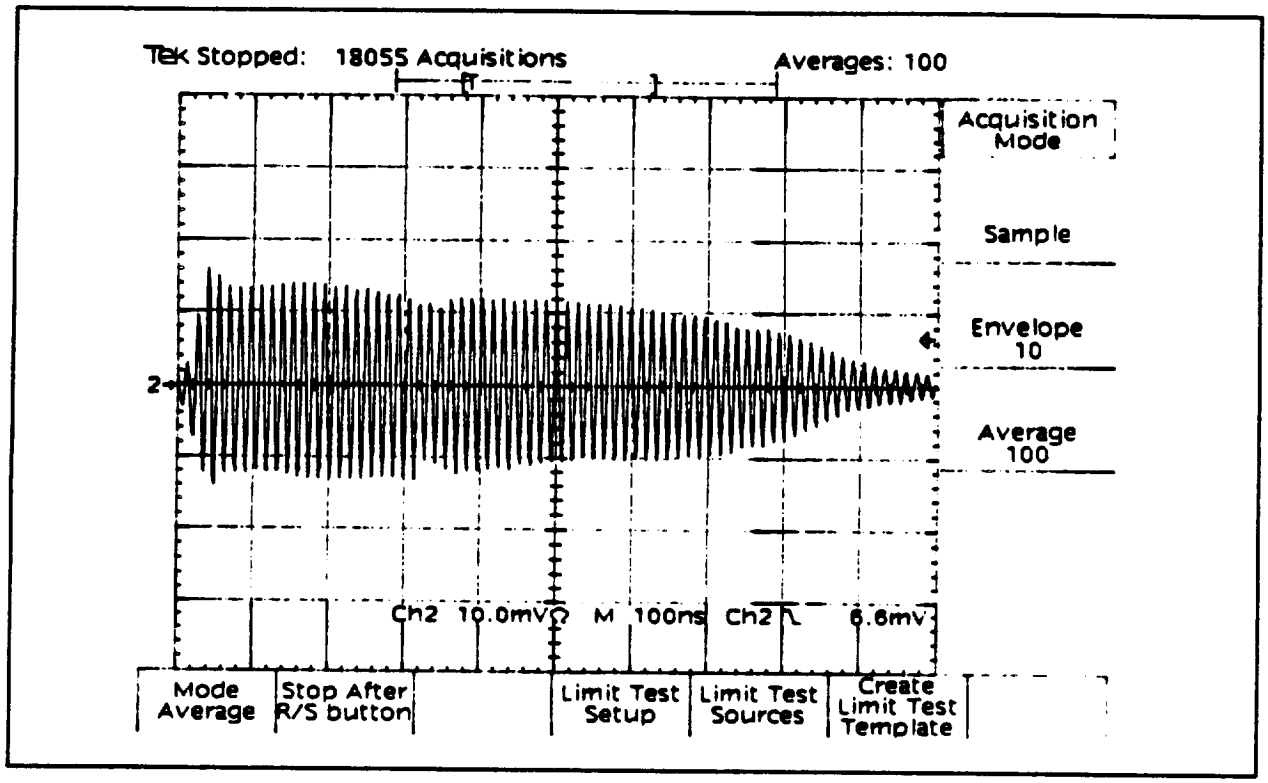


Figure 6: Measured impulse response of a 160-tap HACT device.

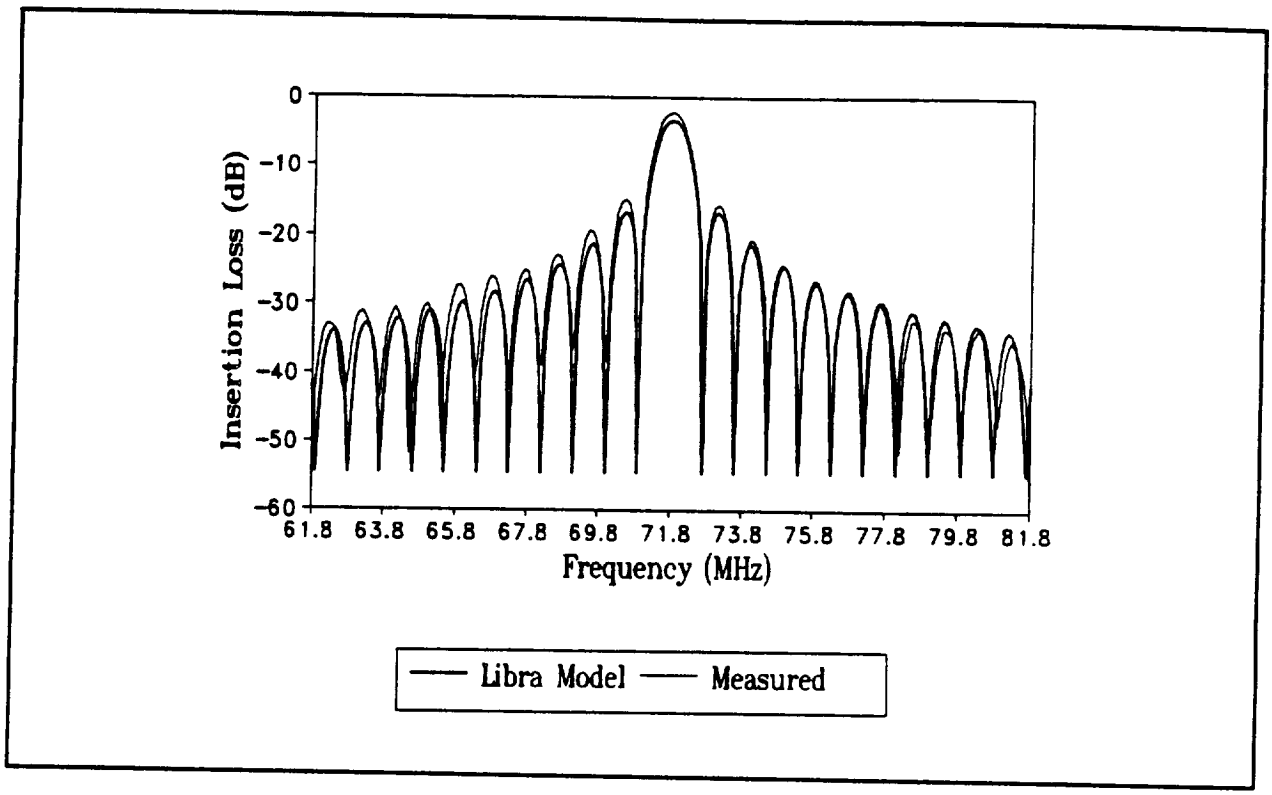


Figure 7: Measured and simulated frequency response of a 160-tap HACT device.

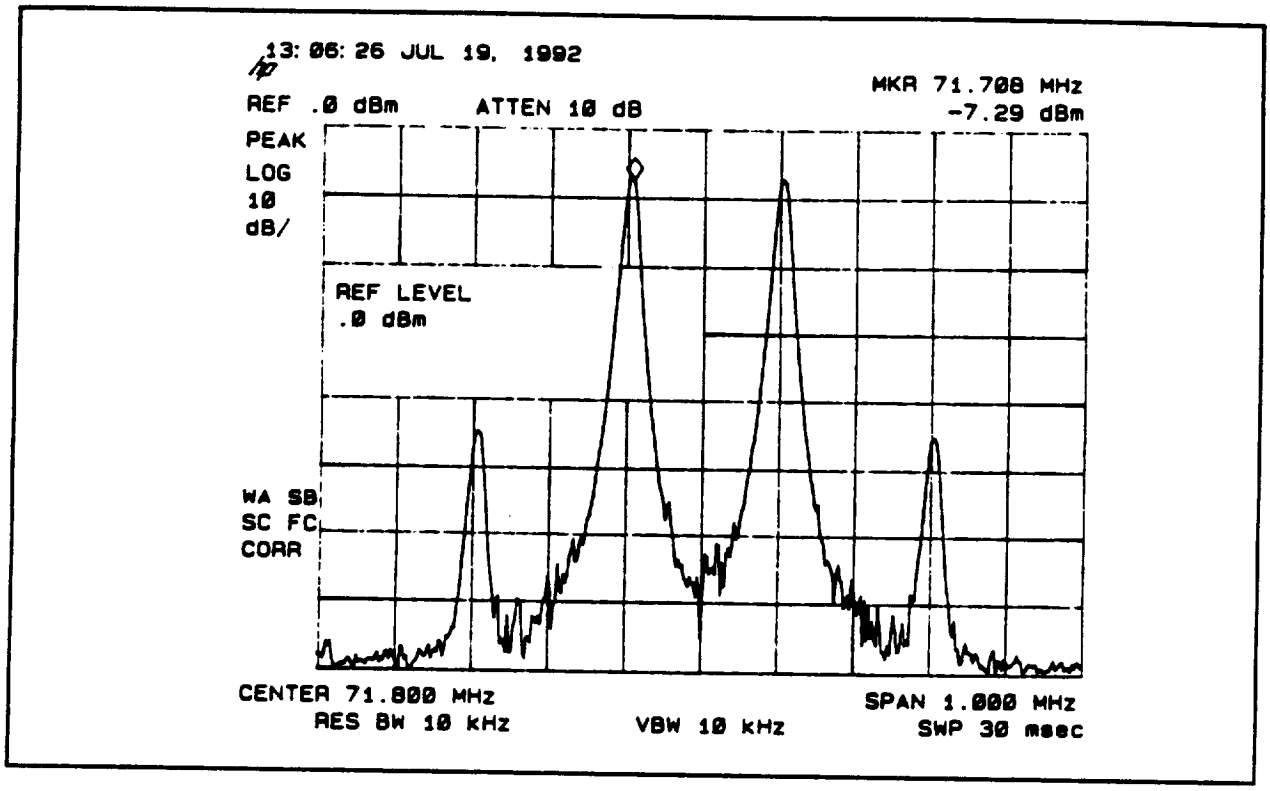


Figure 8: Measured intermodulation distortion of a 160-tap HACT device.

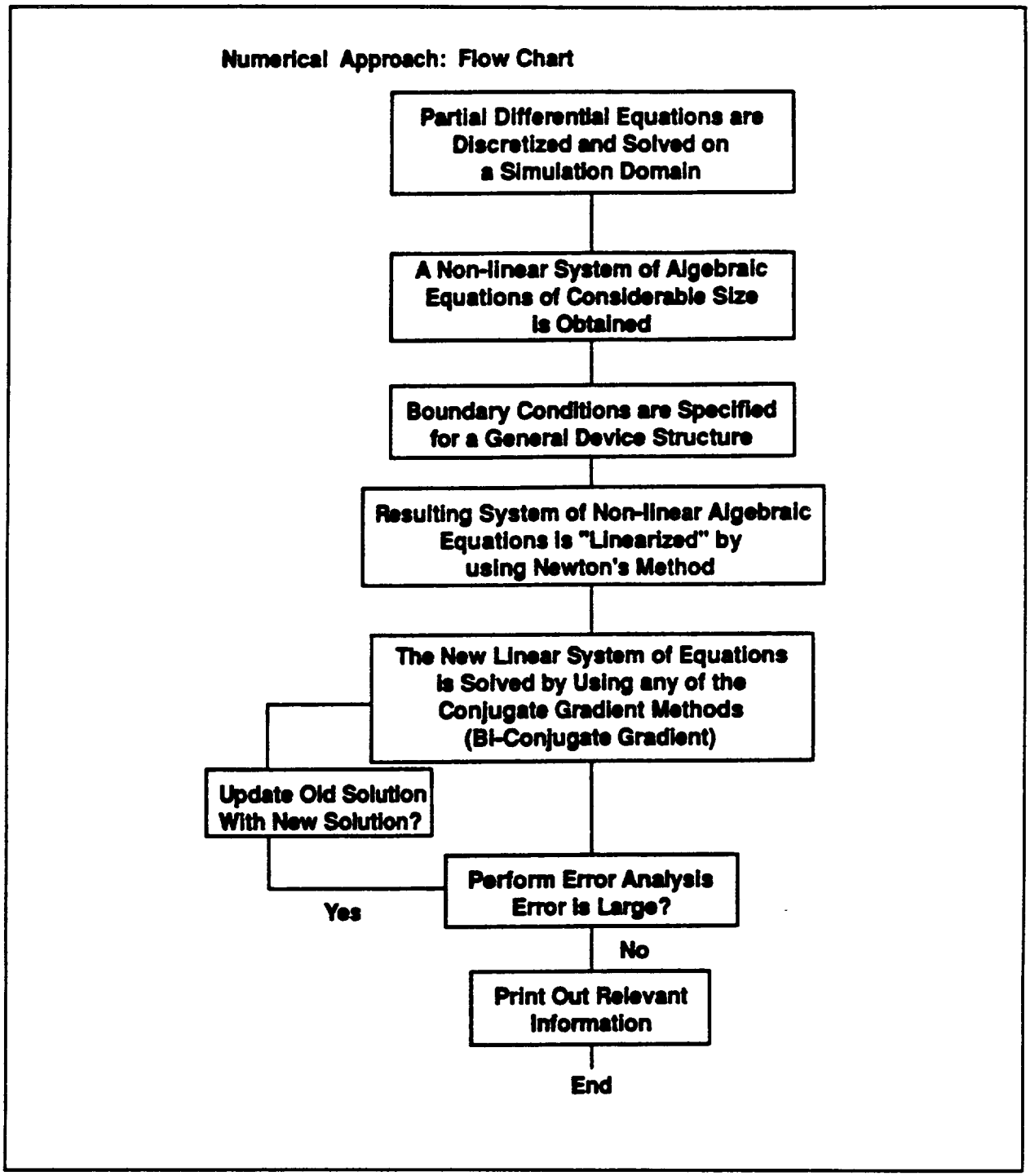


Figure 9: Flowchart illustrating how the numerical simulation of the transistor is structured.

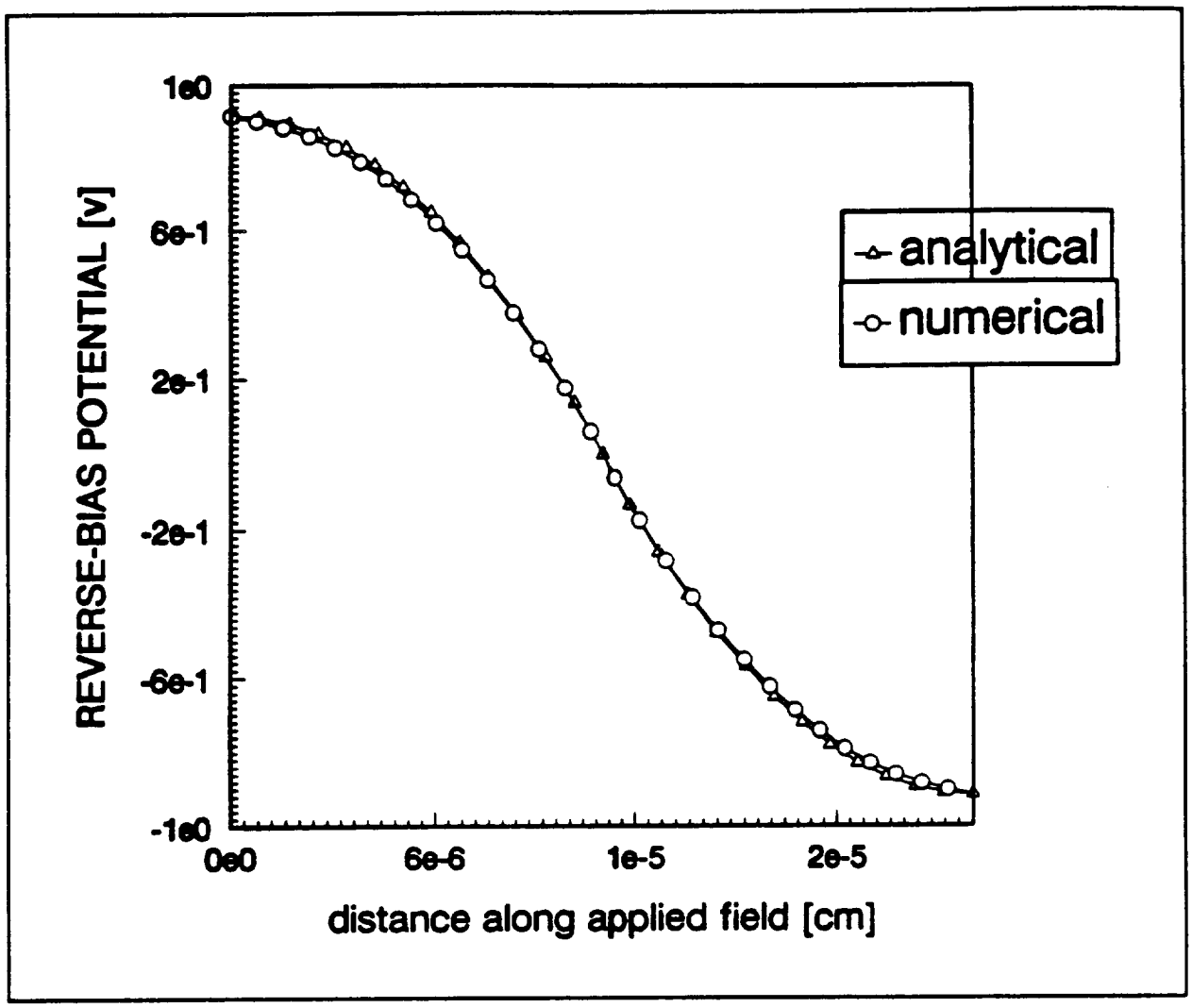


Figure 10: Plot of the calculated reverse bias potential as a function of distance within the depletion region of a p-n junction diode. Comparison of the numerical solution to the standard 1-dimensional depletion approximation (analytic model) is made. Excellent agreement between the two approaches is found.

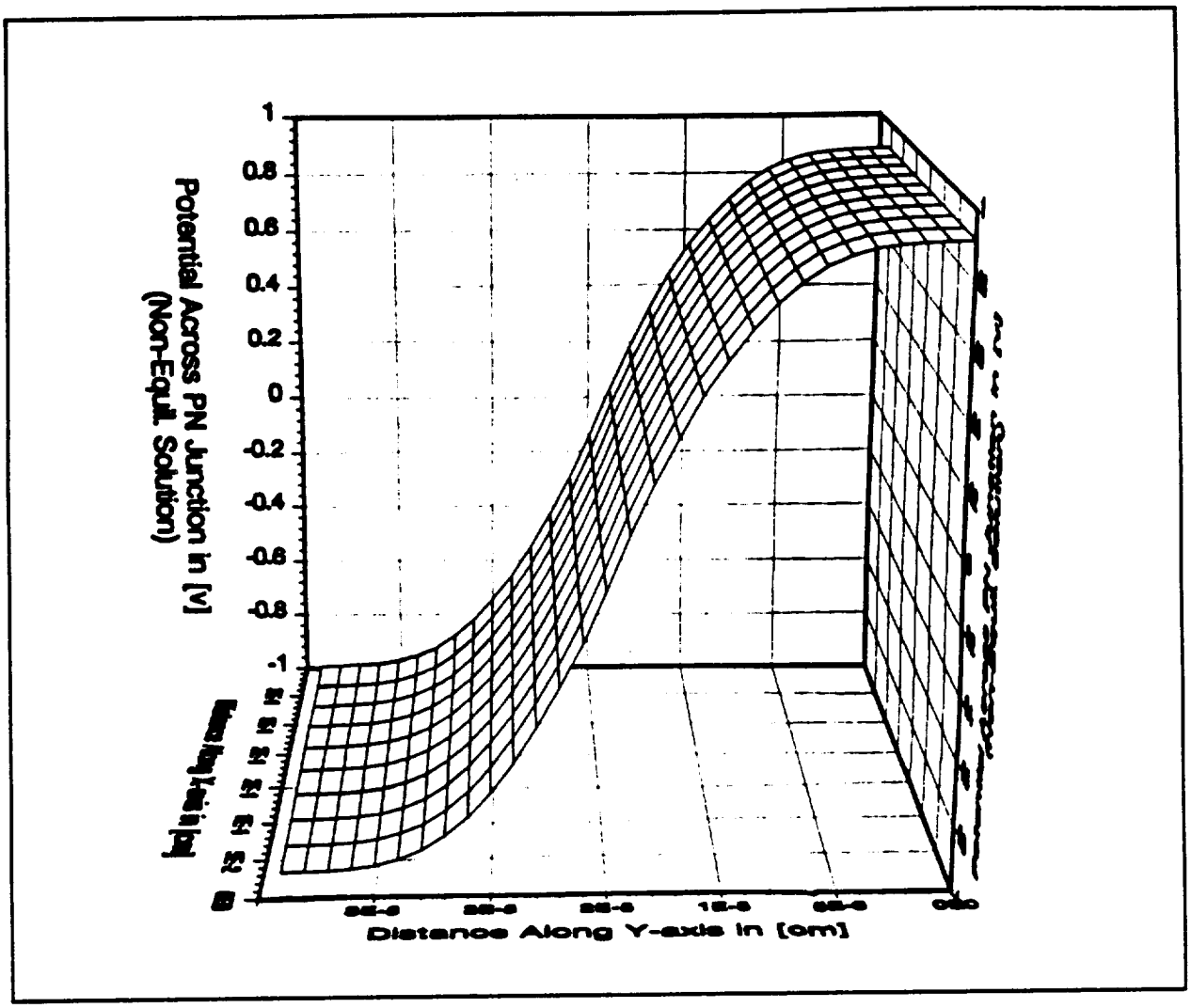


Figure 11: Two-dimensional plot of the calculated reverse bias potentential as a function of distance along the depletion region (y axis).

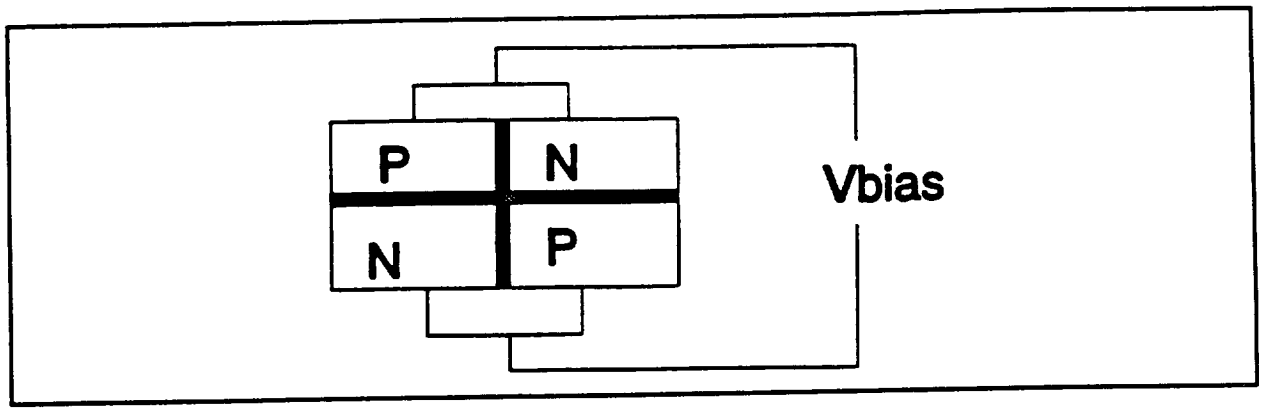


Figure 12: Test device number 2. The device consists of two p-n homojunctions arranged as shown in the diagram. The materials system examined is GaAs.

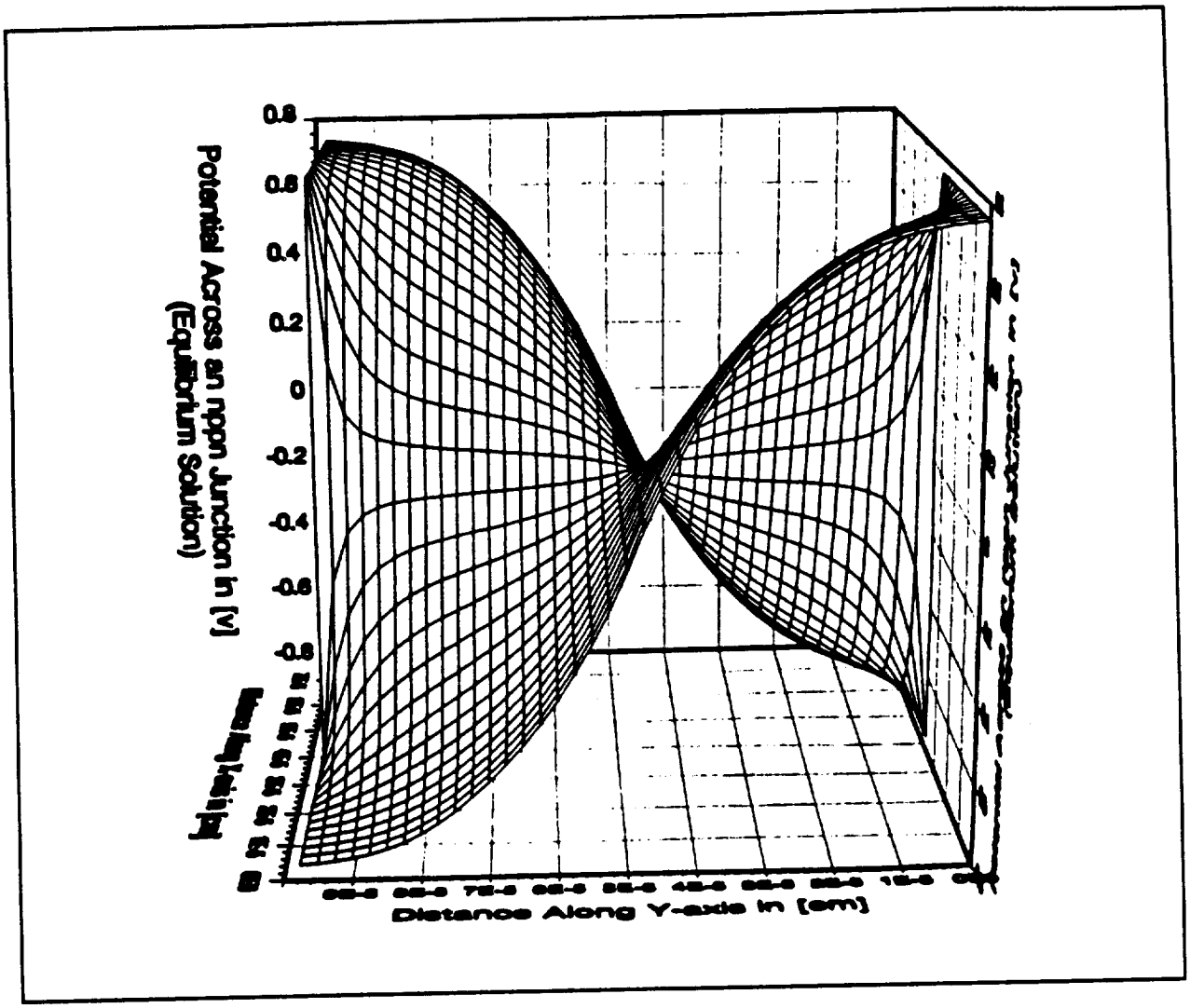


Figure 13: Plot of the calculated potential for test device number 2 under equilibrium conditions.

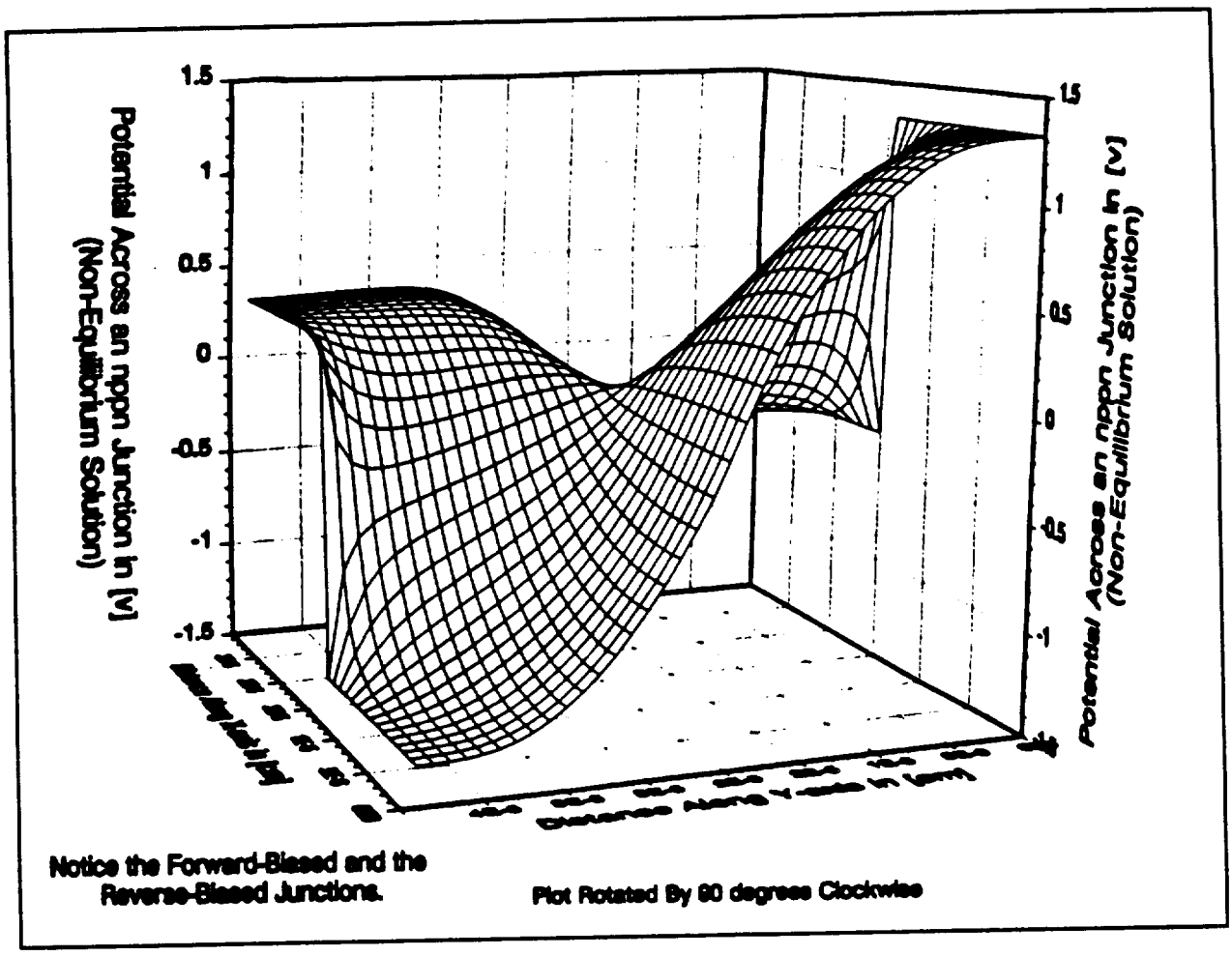


Figure 14: Plot of the calculated potential for test device number 2 under reverse biased conditions. Comparison of Figures 13 and 14 shows greater band bending in reverse bias.

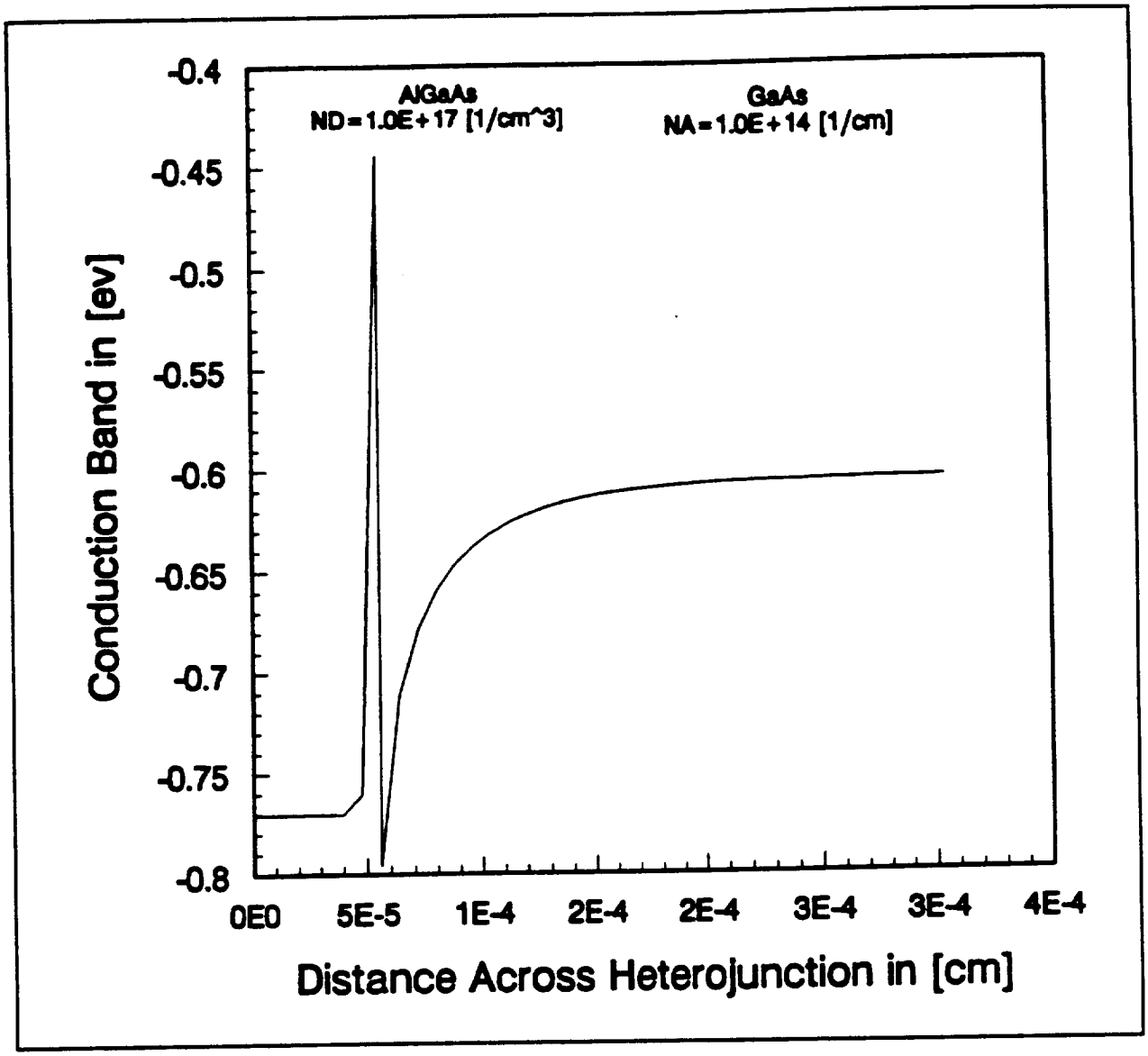


Figure 15: Calculated conduction band bending for a GaAs/AlGaAs heterojunction doped as shown in the diagram. The band edge discontinuity is assumed to be 62% of the energy gap in accordance with the best known experimental estimates.

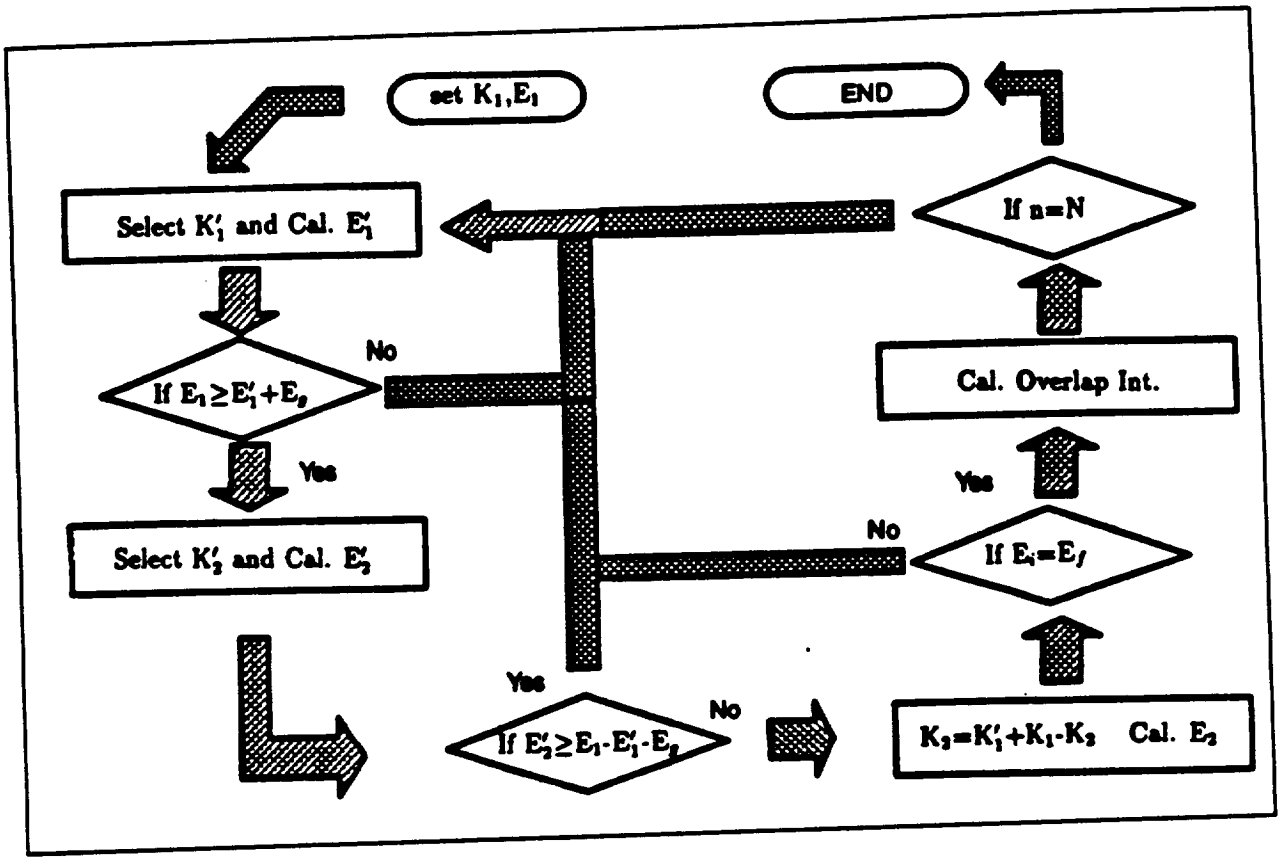


Figure 16: Flowchart depicting the procedure by which the impact ionization transition rate is calculated.

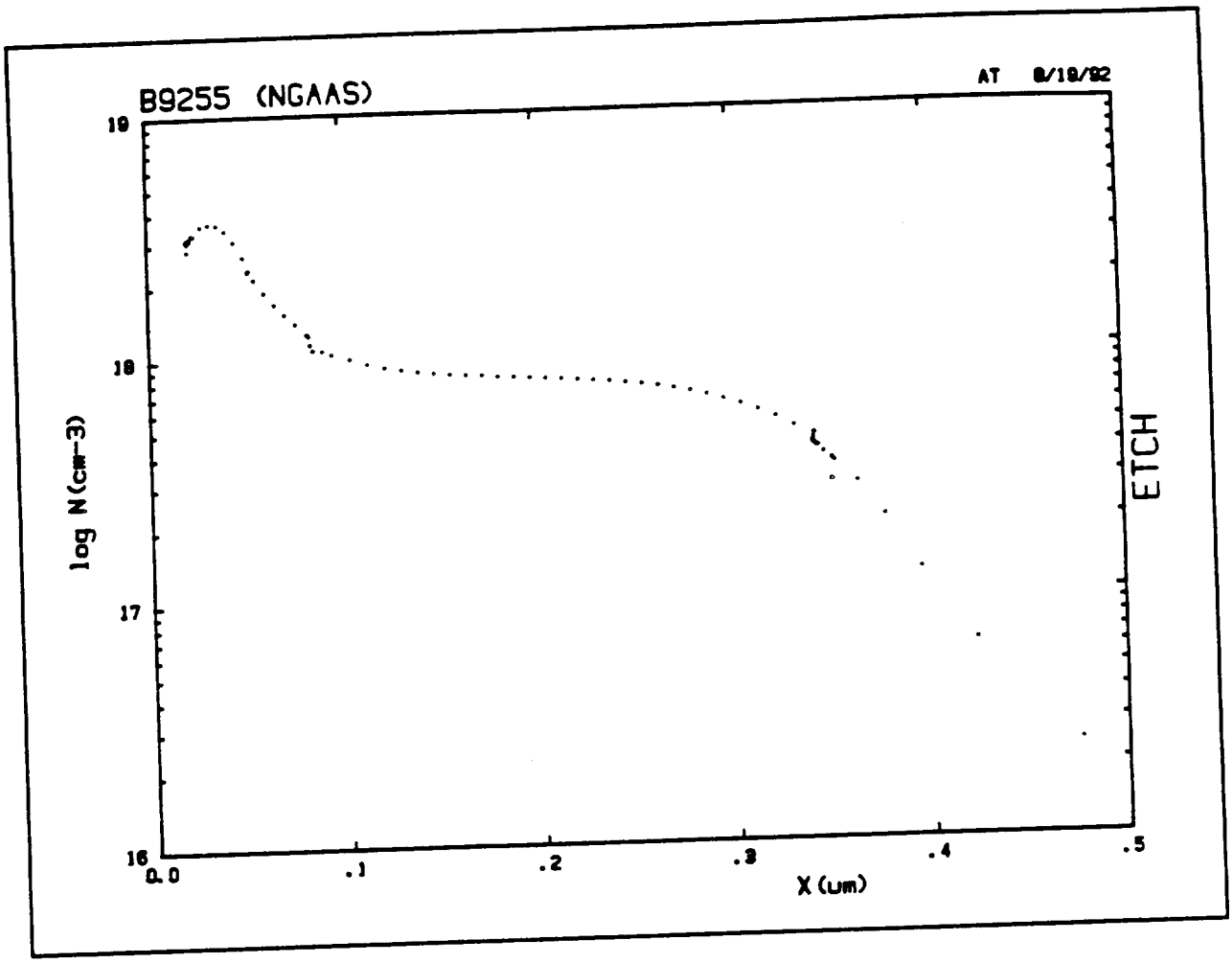


Figure 17: Carrier concentration profile of sample B92-55 as measured by the polaron technique.

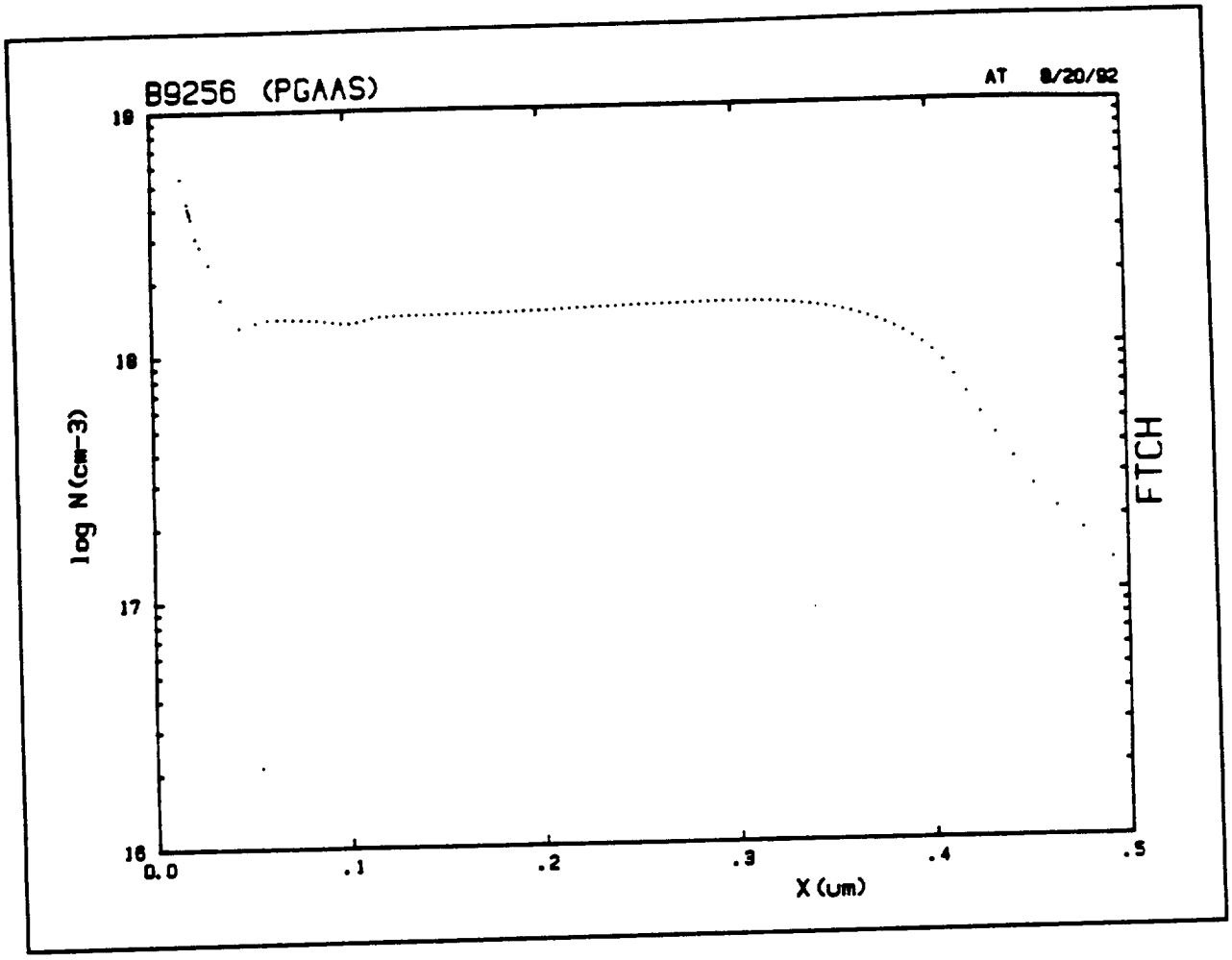


Figure 18: Carrier concentration profiles of sample B92-56 as measured by the polaron technique.

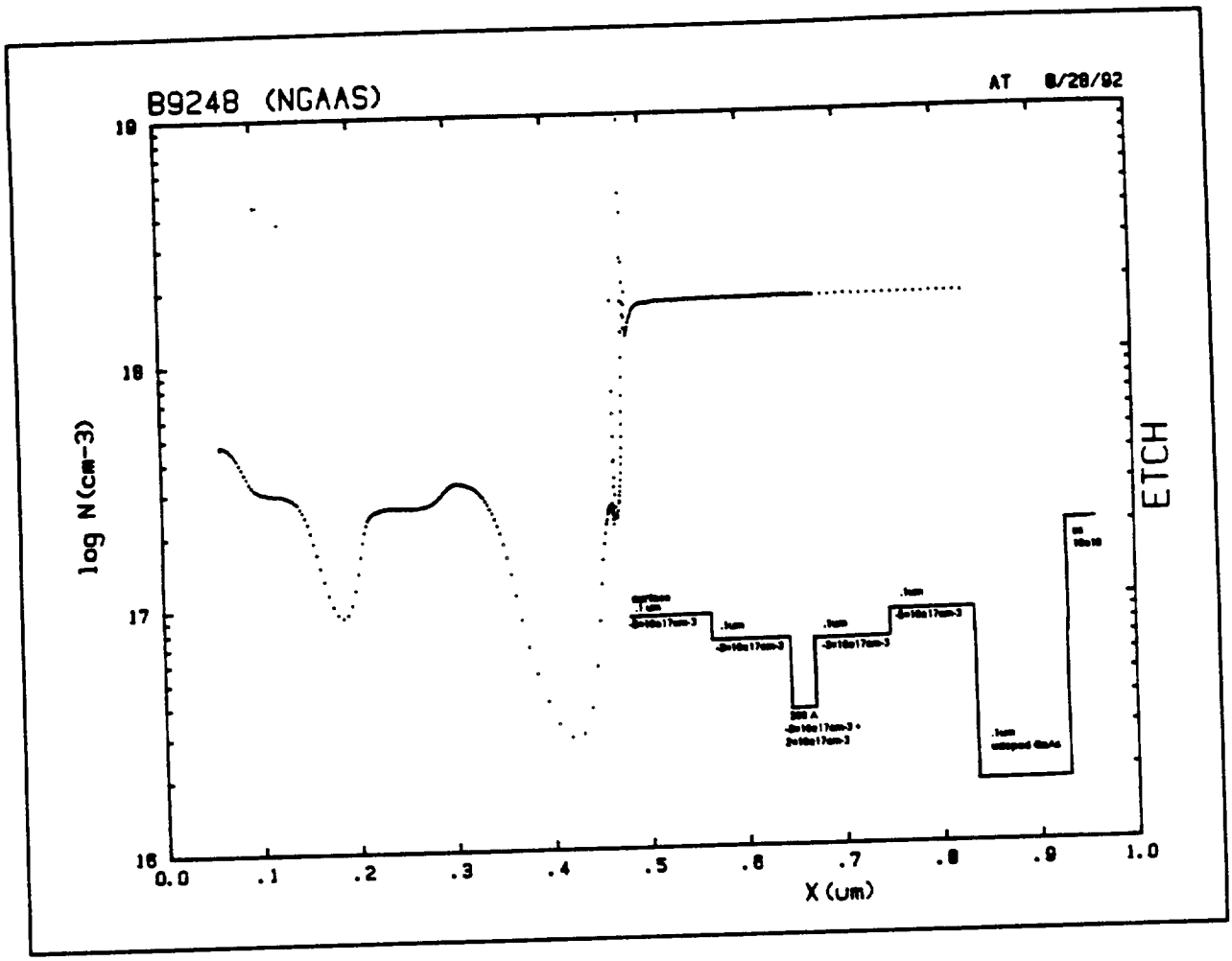


Figure 19: Layer structure and polaron evaluation of sample B92-48.

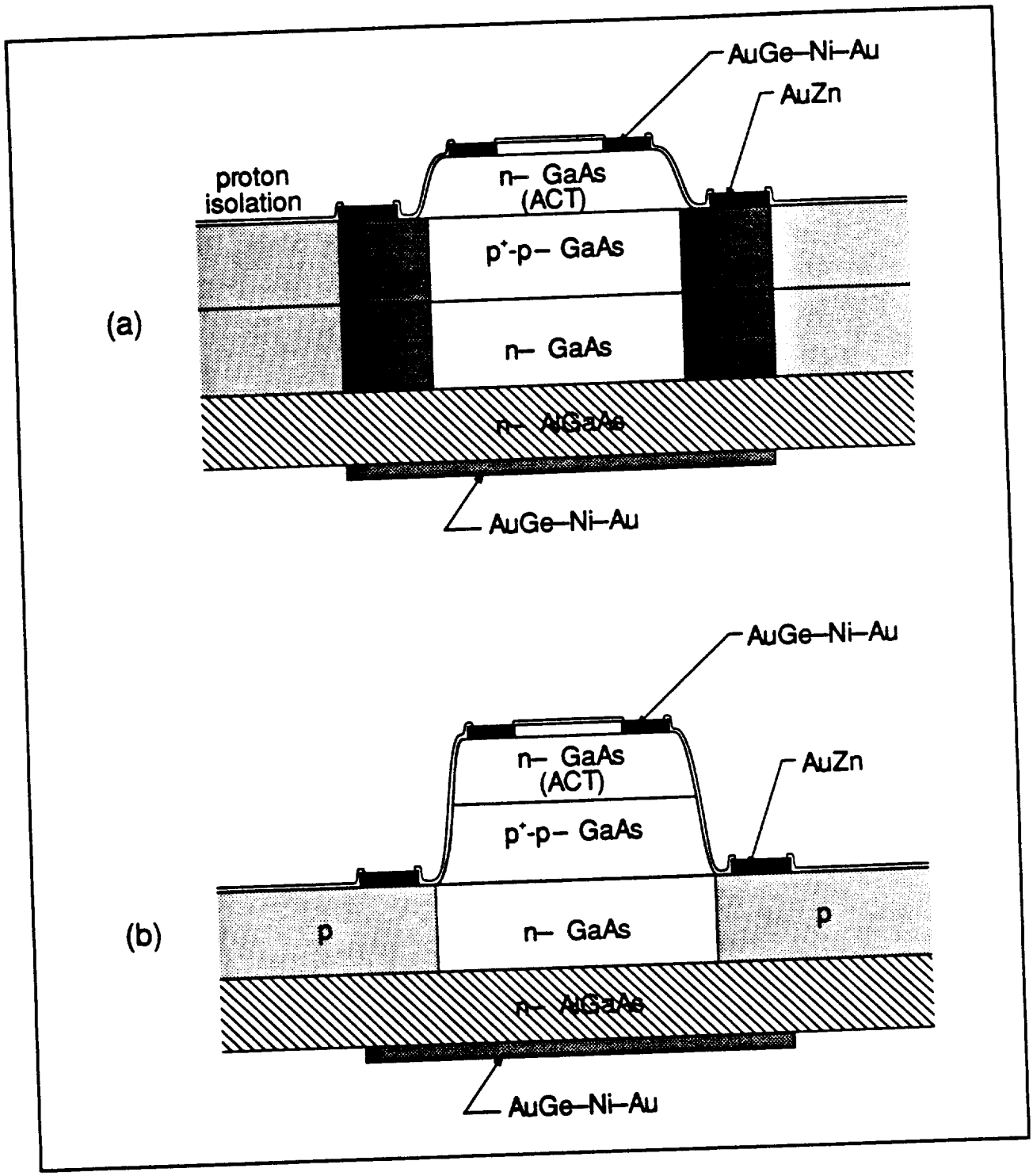


Figure 20: Proposed designs for charge transfer and overflow transistors.

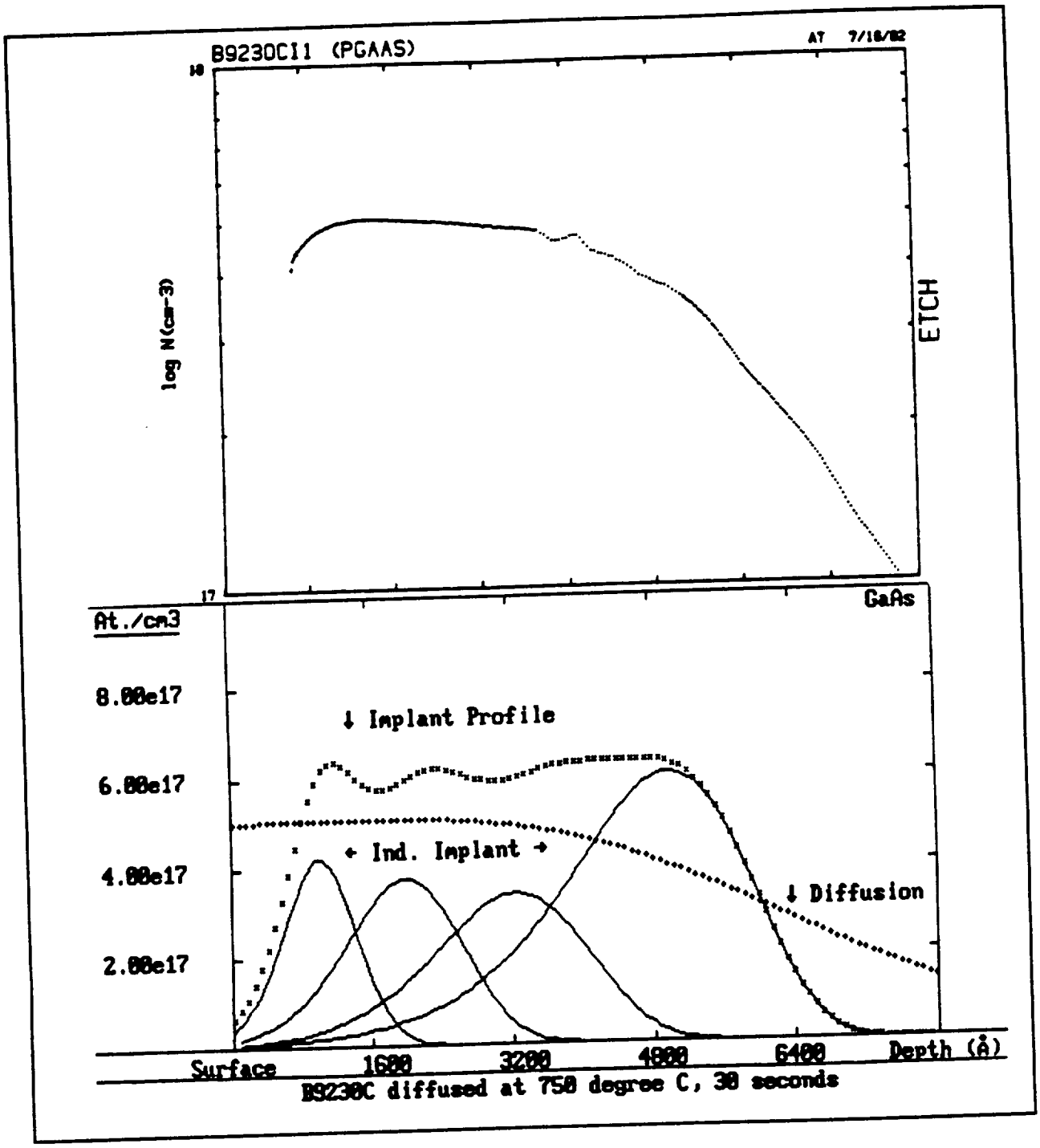


Figure 21: (a) Experimental polaron profiles measured for a Be implanted and annealed sample and (b) theoretical profile for same sample.

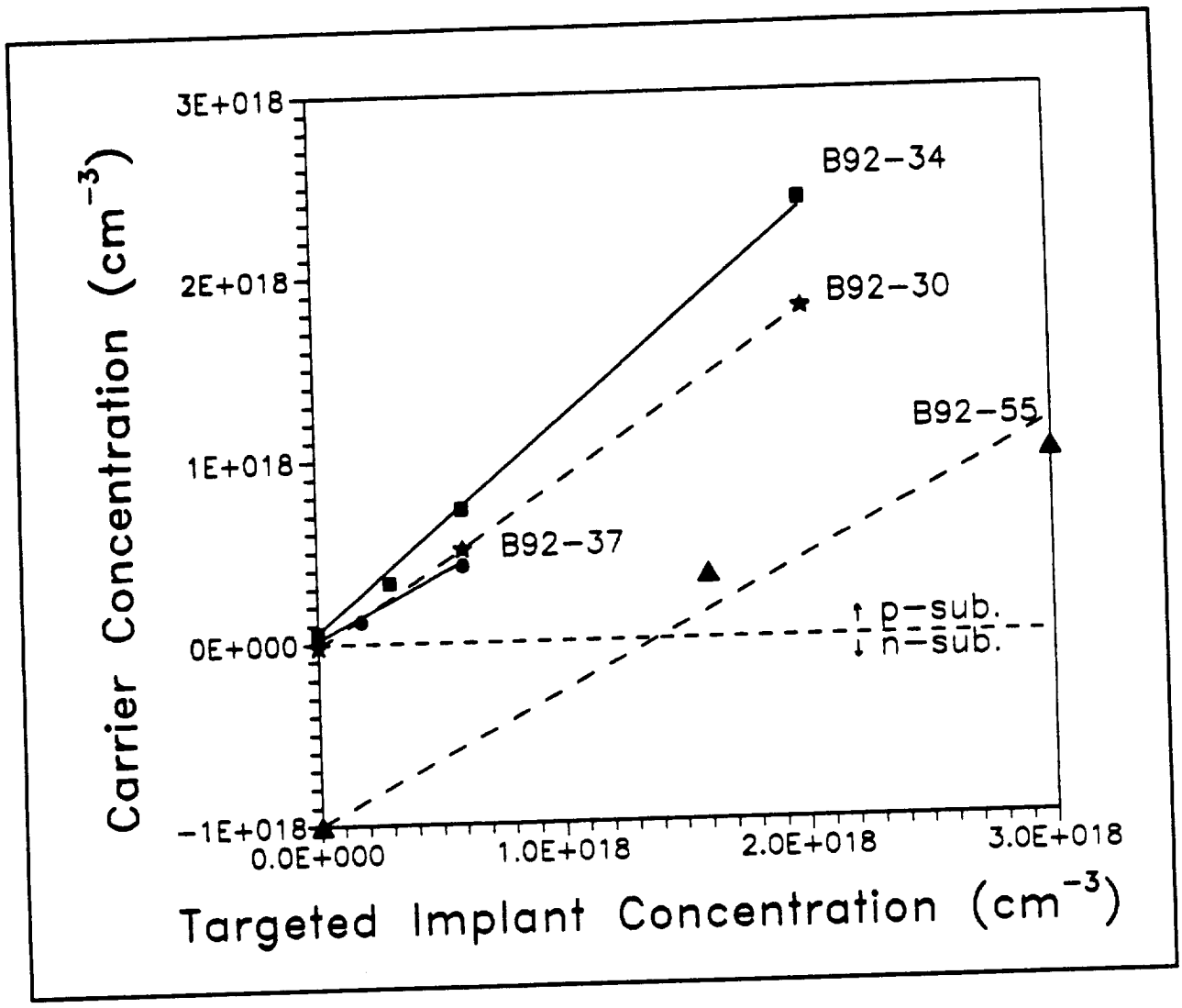


Figure 22: Carrier concentration versus target implanted concentration for n- and p-type doped GaAs layers.

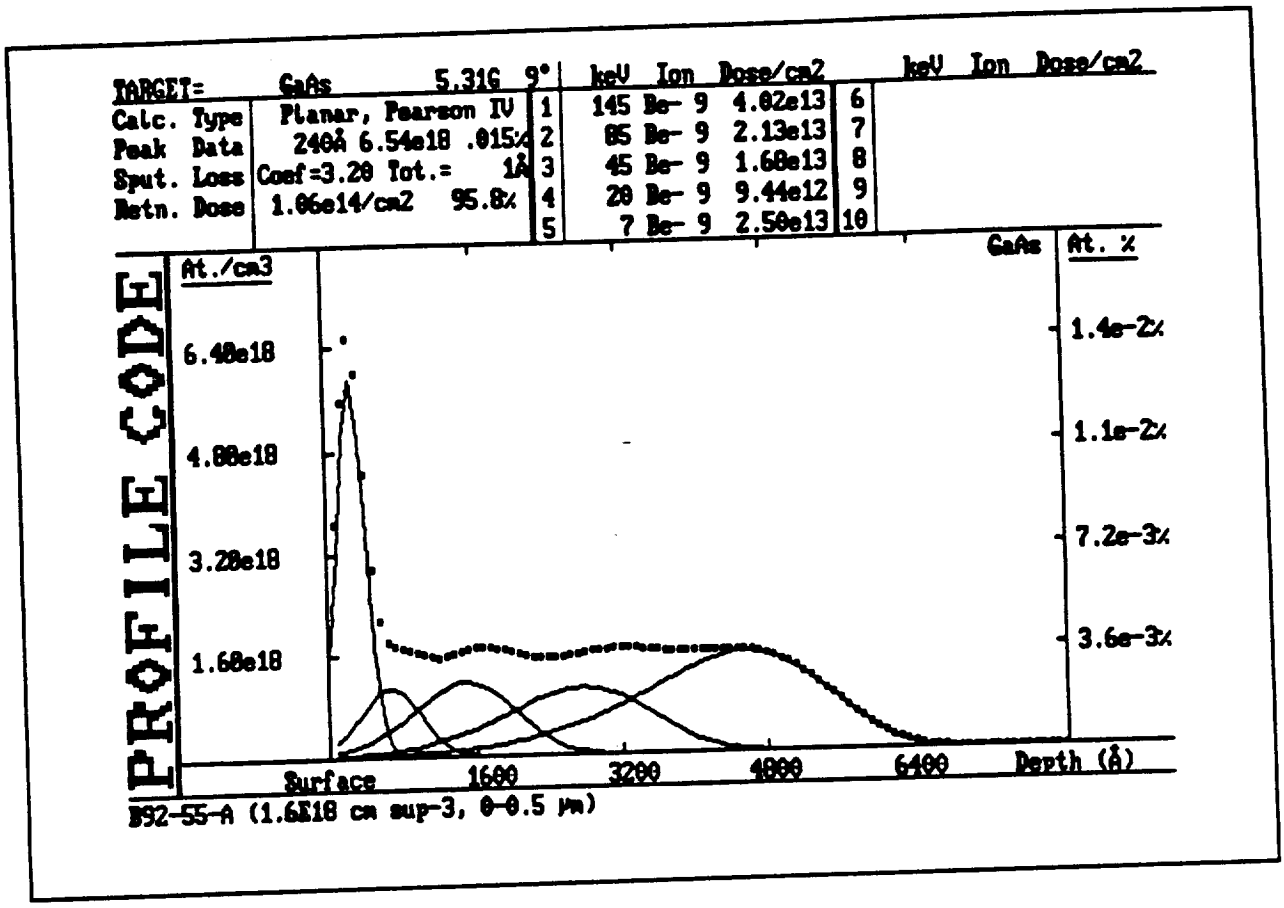


Figure 23: Theoretical implant profile for sample B92-25 showing $p^+$-surface profile.

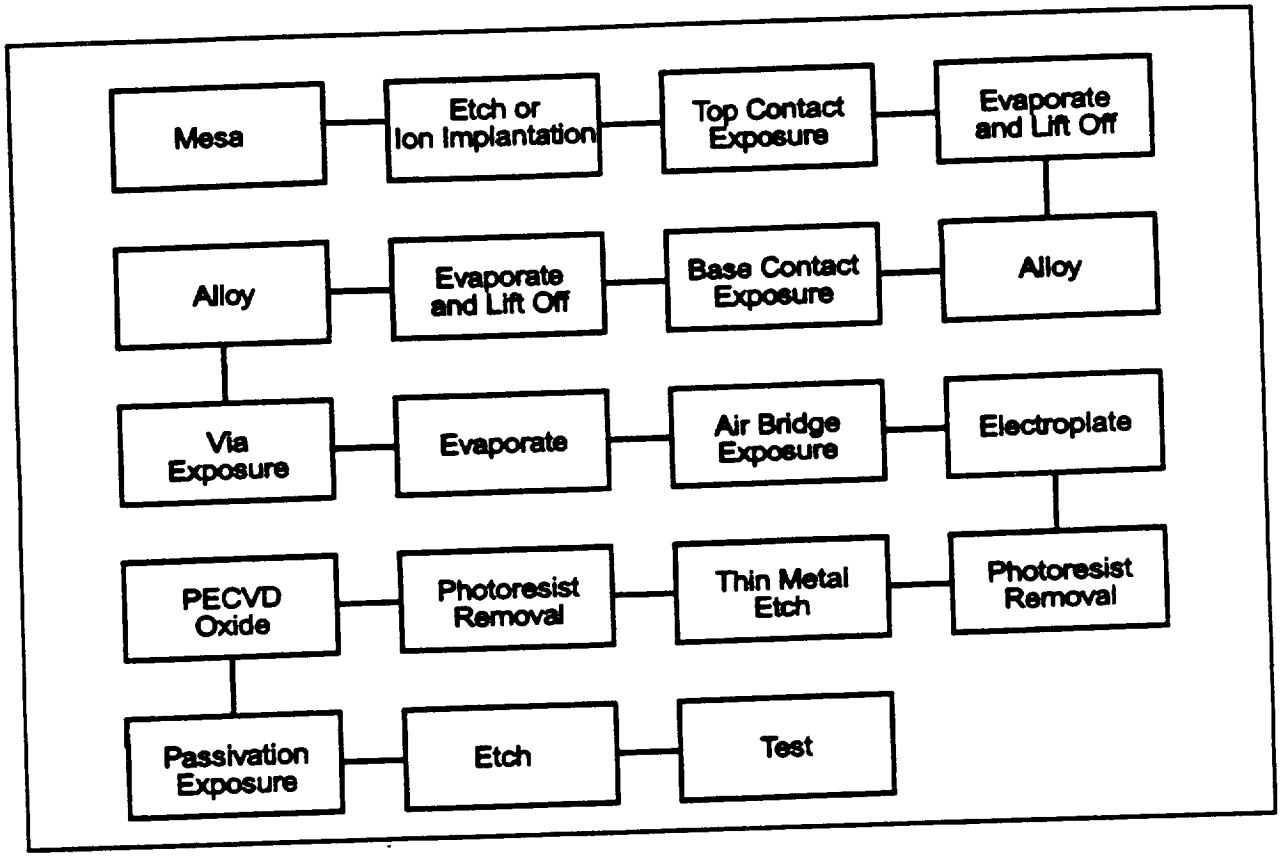


Figure 24: Process flow diagram for fabricating charge transfer and overflow transistor.